University of Tartu

Faculty of Science and Technology

Institute of Technology

Laur Edvard Lindmaa

Development of modular Electrical Power System for KuupKulgur prototype

Master's thesis (30 ECTs)
Robotics and Computer Engineering

Supervisors: Quazi Saimoon Islam, M.Sc.

Assoc. Prof. Dr. Mihkel Pajusalu

Tartu 2025

Abstract/Resümee

Development of modular Electrical Power System for KuupKulgur prototype
CubeRovers are a new class of lightweight, modular robotic platforms designed to lower the barrier to lunar surface exploration. To support such systems, a reliable and modular Electrical Power System (EPS) is essential. This thesis focuses on the development of an EPS for KuupKulgur, a CubeRover prototype created at Tartu Observatory. An advanced EPS-v2 was designed to meet a comprehensive set of power and communication requirements. While EPS-v2 serves as the foundation for future implementations, a simplified EPS-v1.1 was subsequently developed based on lessons learned during the design of v2. This version was tailored to enhance the reliability and performance of the current KuupKulgur rover prototype. The work includes the design, prototyping, and testing of both EPS boards. All system requirements were fulfilled, with the exception of hot-swappability, which was deprioritized due to mechanical and reliability constraints. Although space qualification was beyond the scope of this thesis, the system architecture allows for potential future thermal-vacuum and radiation testing. The results presented here lay the groundwork for future EPS revisions compatible with CubeRover standards and operational lunar missions.

CERCS: T120 Systems engineering, computer technology; T171 Microelectronics; T320 Space technology[1]

Keywords: KuupKulgur, CubeSat, On-board computer, CubeRover, Electronics

Toitealamsüsteemi arendamine KuupKulguri prototüübile CubeRoverid on uue põlvkonna kerged ja modulaarsed robotplatvormid, mille eesmärk on vähendada tehnilisi ja rahalisi takistusi Kuu pinnale suunatud uurimismissioonide läbiviimisel. Nende süsteemide töökindlaks toimimiseks on vajalik usaldusväärne ja modulaarne elektritoitesüsteem (EPS). Käesolev magistritöö keskendub Kuupkulguri EPS-i arendamisele. KuupKulgur on Tartu Observatooriumis arendatav CubeRoveri prototüüp. EPS-v2 projekteeriti vastavalt KuupKulguri meeskonna poolt eelnevalt kokku lepitud toite- ja sidestandarditele. Selle arenduse käigus saadud kogemuste põhjal töötati välja ka lihtsustatud versioon EPS-v1.1, mille eesmärk oli parandada olemasoleva KuupKulguri prototüübi töökindlust ja efektiivsust. Töö raames käsitletakse mõlema toitesüsteemi arendust ja katsetamist. Kõik süsteemi nõuded täideti, välja arvatud akude kuumvahetus, mis jäeti rakendamata mehaaniliste piirangute ja töökindluse kaalutlustel. Kuigi kosmosekeskkonna testid ei kuulunud selle töö fookusesse, on süsteemi arhitektuur kavandatud nii, et tulevikus oleks võimalik läbi viia termovaakumi- ja kiirguskindluse katsed. Töö tulemused loovad aluse CubeRoveri standarditele vastavate toitealamsüsteemide edasiseks arendamiseks ning aitavad valmistuda tulevasteks kuumissioonideks.

CERCS: T120 Süsteemitehnoloogia, arvutitehnoloogia; T171 Mikroelektroonika; T320 Kosmosetehnoloogia[1]

Märksõnad: KuupKulgur, Kuupsatelliit, Pardaarvuti, CubeRover, Elektroonika

Contents

List of figures

Acronyms

ADC Analog-to-Digital Converter. 15–18, 22, 24, 48

CAN Controller Area Network. 14, 16, 36

COTS Commercial off-the-shelf. 14

EPS Electrical Power System. 2, 6, 8, 10–18, 20, 21, 23–27, 29–37, 43, 48, 70

ESD Electrostatic discharge. 23

GPIO General-purpose input/output. 18

HSMCI High-speed Multimedia Card Interface. 19

IC Integrated Circuit. 12, 17, 19–21, 30, 31, 35, 36

IMU Interial Measurement Unit. 11, 32

LEO Low Earth Orbit. 10

MCU Microcontroller Unit. 6, 15, 17–20, 24, 48

MOSFET Metal–Oxide–Semiconductor Field-Effect Transistor. 22

MPB Main Power Bus. 6, 15, 16, 34, 48

NASA National Aeronautics and Space Administration. 8, 39

NTC Negative Temperature Coefficient. 21, 24

OBC On-Board Computer. 18, 36

PCB Printed Circuit Board. 15, 16, 21–24

PCIe Peripheral Component Interconnect Express. 16, 17, 36

SPI Serial Peripheral Interface. 14, 16–18, 24, 36

TID Total Ionizing Dose. 14

USB-C Universal Serial Bus Type-C. 11, 15, 16, 19, 20, 30, 31, 48

1 Introduction

In recent years, the global focus on lunar exploration has surged once again, driven by major initiatives such as National Aeronautics and Space Administration (NASA)'s Artemis program and the planned Lunar Gateway [2, 3]. These efforts signal a renewed international race to the Moon, with an emphasis on sustained presence, scientific research, and infrastructure development. As part of this momentum, compact robotic rovers have emerged as critical platforms for surface operations, such as mapping, scouting, and technology demonstration. These small-scale lunar rover prototypes demand highly efficient and reliable EPS systems capable of withstanding the Moon's harsh thermal and radiation environments. KuupKulgur, a student-developed rover at Tartu Observatory, serves as a testbed for such systems, enabling rapid iteration and validation in analogue environments.

This thesis focuses on the design, development, and testing of EPS-v2, a modular and more efficient successor to the original EPS that has been developed for the existing KuupKulgur testing platform. The aim is to address key limitations in the earlier version, including thermal issues, limited current-handling capacity, and integration challenges. Additionally, the lessons learned during the development of EPS-v2 were then applied in the redesign of EPS-v1.1, a drop-in replacement for the original EPS that retains the same mechanical form factor as EPS-v1 while benefiting from the architectural and efficiency improvements introduced in EPS-v2.

1.1 CubeRovers

To guide standardization and promote payload interoperability, the concept of the CubeRover has emerged as a scalable framework for small, modular lunar rovers. Similar in spirit to CubeSats, CubeRovers are designed around standardized form factors and mechanical, electrical, and software interfaces to lower the entry barrier for lunar surface missions. The KuupKulgur rover prototype falls within this category, specifically aligning with the 2U CubeRover standard in terms of physical dimensions.

The CubeRover standard, developed and promoted by Astrobotic in collaboration with NASA, provides documentation on size classifications, connector placements, electrical interfaces, and general system-level requirements [4]. KuupKulgur does not aim to be fully compliant in every aspect, but the design choices, especially the modular EPS, are informed by the same philosophy of reusability and standardization. This alignment supports potential integration with lunar delivery platforms and compatibility with future development ecosystems.

1.1.1 KuupKulgur

KuupKulgur is a student-developed CubeRover prototype created at the Tartu Observatory as part of a broader effort to contribute to the new wave of lunar exploration initiatives. Inspired by the modular standards proposed for CubeRovers, KuupKulgur is designed to follow the general guidelines of compact, scalable, and lightweight robotic platforms for planetary surface exploration, while remaining adaptable for terrestrial testing and educational purposes.

The rover is developed to fit within the 2U CubeRover form factor and features a modular architecture that allows for the easy replacement and testing of key subsystems, such as power, mobility, and data acquisition. Currently, its primary purpose is to act as a testbed for validating technologies and operational concepts in lunar-analogue environments. A special emphasis is placed on gathering performance data in extreme conditions, such as those encountered in space, which mimic the harsh environment on the Moon. While KuupKulgur is not intended for immediate flight use, its design philosophy follows the principles set forth by the CubeRover movement. The most recent version of the KuupKulgur prototype can be seen in Figure 1.

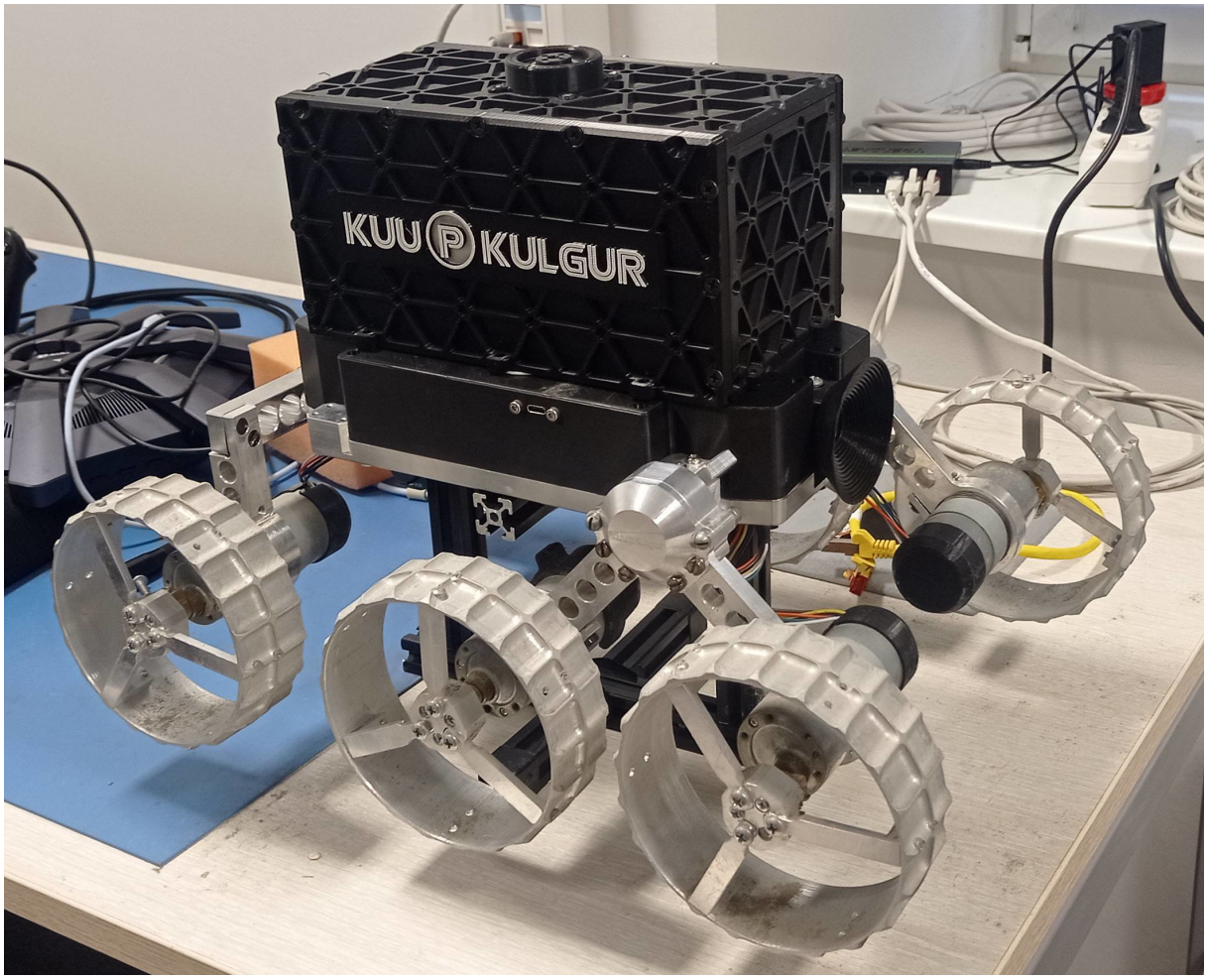


Figure 1: Current revision of KuupKulgur in the Integration Laboratory

2 Literature review

Although interest in lunar exploration has resurged in recent years, especially with the Artemis program and international lunar initiatives, actual surface missions remain limited. As a result, there is a noticeable scarcity of up-to-date, reliable sources specifically related to lunar surface operations and power system performance under real lunar conditions.

Moreover, since no CubeRover has yet completed a lunar surface mission, there is no publicly available flight heritage data to validate the standard's assumptions under actual lunar conditions. This includes extreme thermal cycling, radiation exposure, abrasive regolith, and limited sun exposure, all factors that impose stringent requirements on power systems.

Given these constraints, developers often turn to CubeSat EPS designs as a reference point. CubeSats have undergone extensive development and validation in Low Earth Orbit (LEO) and offer well-documented approaches to power generation, regulation, and energy storage in compact form factors [5]. While CubeSat EPS systems are not directly designed for lunar use, they provide a practical and scalable starting point for rover developers. By adapting these systems, they can serve as effective prototypes or early-stage solutions for lunar rovers, including CubeRovers.

2.1 Known limitations

Small-scale lunar systems like CubeRovers face a range of inherent limitations due to their compact size and potential strict mass budgets. One of the most critical challenges is limited surface area for solar power generation, which directly affects available energy and mission duration. Their small thermal mass makes them highly susceptible to extreme temperature swings on the Moon, where surface temperatures can fluctuate by over 250°C between lunar day and night [6]. Additionally, miniaturized electronics must still meet the same radiation and vacuum survivability standards as larger spacecraft, which can be difficult to achieve with off-the-shelf components. There is also a lack of redundancy in many subsystems due to space constraints, making them more vulnerable to single-point failures. Furthermore, dust mitigation becomes a pressing issue, as the negatively charged fine lunar regolith can interfere with mechanical parts and electrical connectors, especially when there is less room for protective shielding or sealing [7]. Collectively, these constraints place a high premium on efficient, integrated subsystem design, particularly for power systems, which must remain lightweight while still being robust and autonomous enough to support mobility and communication under lunar surface conditions.

3 Related work

As related work, the author could only take inspiration from KuupKulgur's previous models and Astrobotics' limited specifications.

3.1 Existing architectures

The current KuupKulgur prototype employs an architecture centered around the NVIDIA Jetson Orin Nano, which serves as the main onboard computer [8]. This is connected to a custom splitter board that adapts the Jetson's interface to a Raspberry Pi-compatible pinout, enabling seamless integration with both the payload systems and the main communication bus [9]. The main bus stack presently includes two boards: the EPS-v1 on the top layer and the motor control board beneath it. Positioned adjacent to this stack is the battery board, which houses five 18650 Li-ion cells configured in series. The complete architecture of EPS-v1 can be found in Appendix B.

3.1.1 EPS-v1

The EPS-v1 consists of several submodules within a single board:

- Universal Serial Bus Type-C (USB-C) Power Delivery input
- 24 V step-up switching regulator
- Battery charging and balancing circuitry
- PowerPath controller
- 3.3 V, 5 V, and 12 V step-down switching regulators
- Interial Measurement Unit (IMU)

Although the EPS-v1 includes an IMU, this component is arguably misplaced, as it is not logically part of the power system and is not present elsewhere in the rover. Its inclusion on the EPS board was a convenience choice during prototyping rather than a result of architectural necessity. Render of the first version of the EPS can be seen in Figure 2. It should be noted that EPS-v1 was also developed by the author prior to the start of the body of this work.

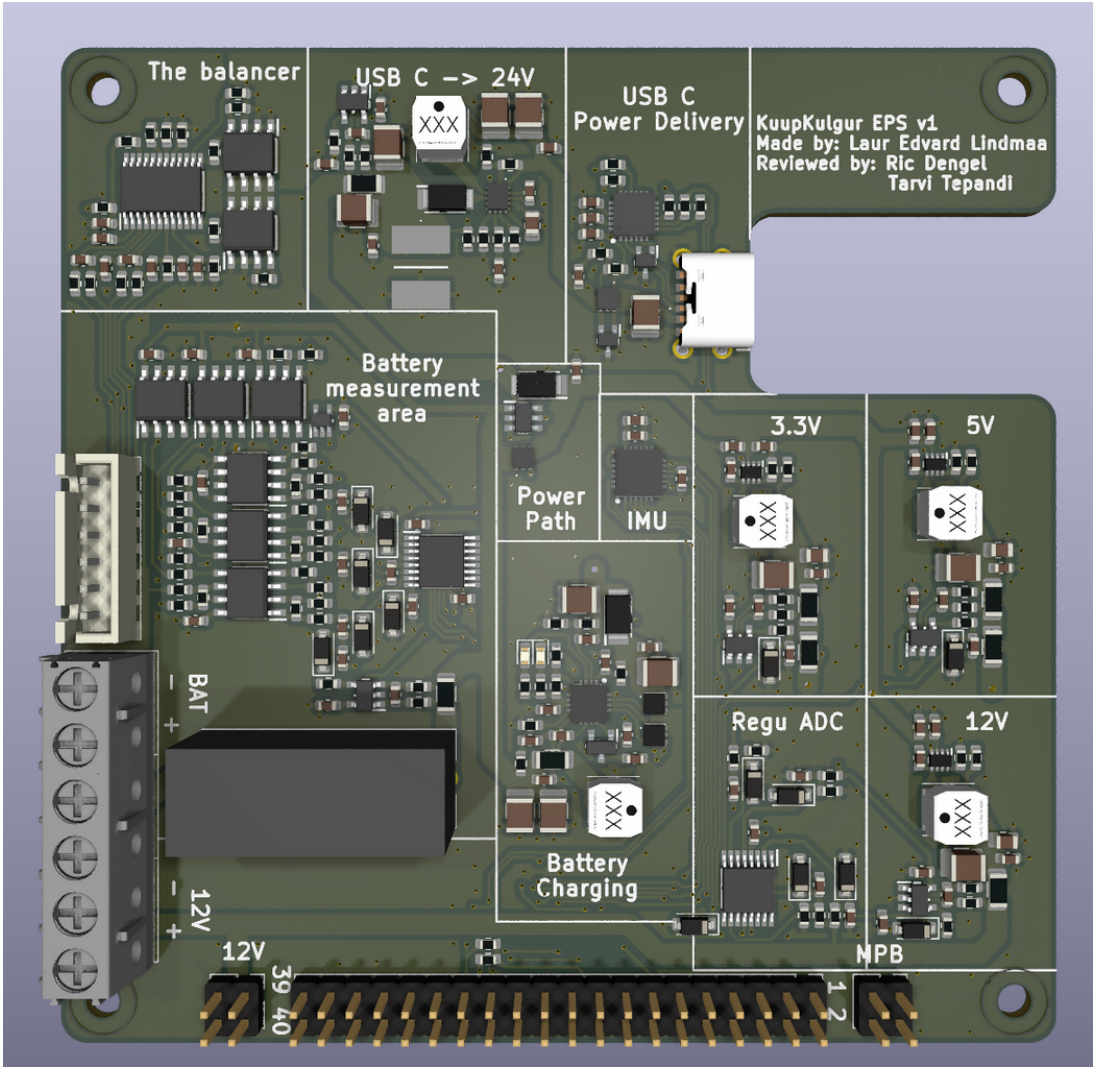


Figure 2: Render of the EPS-v1

3.1.2 Known issues

The first revision of the EPS exhibited several critical issues during operation. One of the primary concerns was the use of suboptimal voltage regulators, specifically the TPS563300, which are rated for a maximum of 3 A and were implemented in a thermally inefficient manner [10]. As a result, internal temperatures of the rover exceeded 70 °C under normal operating conditions. Additional problems were identified in the battery balancing circuitry: the balancer Integrated Circuit (IC) failed to equalize all cells properly, consistently balancing only cells 1–3, while cells 4 and 5 maintained significantly higher voltages. Furthermore, the battery voltage measurement circuit produced noisy data, reducing the reliability of telemetry. The charging module also showed instability, often terminating the charge cycle prematurely, most likely due to thermal issues or excessive imbalance among the cells.

4 Thesis goals

The objective of this thesis is to develop a modular power supply system for the KuupKulgur prototype, select appropriate interfaces, and thoroughly test the complete system. Additionally, collaboration with industry partners is required to identify their specific requirements, which will inform the final design of the rover's power architecture. The objectives of the thesis are as follows:

- Create a new improved EPS for the next revision of KuupKulgur
- Research and select an interface to communicate with the rest of the main stack
- Follow the requirements set by the team and industry partners
- Test the newly designed EPS
- Improve the existing rover prototype EPS

5 EPS-v2 development

In order to develop the EPS-v2, the author took inspiration from the previous EPS version and changed the design to improve total battery capacity and output regulator current capabilities.

5.1 Requirements

The system requirements were based on feedback from KuupKulgur's industry partners and what was agreed on internally by the team. The requirements that were put on the to-be-made EPS were:

Requirement	**Description**
Output Voltages	3.3 V, 5 V, and 12 V regulated outputs with ±10% accuracy
Output Current	5 A per regulator
Temperature	Temperature of the EPS must remain below 80 °C when at maximum required load
Input Source	5-cell lithium-ion battery pack
Battery Protection	Cutoff below 3.0 V per cell with 10 A Fast fuse
Telemetry	Voltage and temperature monitoring per cell
Telemetry	Voltage, current, and temperature monitoring on all voltage regulators
Communication	Serial Peripheral Interface (SPI) interface required, optional Controller Area Network (CAN) support
Modularity	The stack must consist of easily replaceable layers that can be swapped as necessary
Modularity	Batteries have to be hot-swappable to reduce downtime during testing
Form Factor	Compatible with the size constraints shown in Appendix Figure A.

Table 1: EPS System Requirements

It was decided that radiation tolerance is of low priority, as the planned mission duration is at most 14 Earth days. By calculating the estimated Total Ionizing Dose (TID) received during the mission according to the worst-case scenario, it comes out to be around 4 rad, while Commercial off-the-shelf (COTS) electronics tend to survive TID of a few kilorad [11, 12]. Single-event upsets might still be of concern and will have to be investigated in flight-ready hardware.

5.2 New architecture

The updated system architecture consists of two electronic stacks: a central stack housing the EPS and two adjacent battery stacks, each designed with hot-plug capability. A logical schematic of the complete architecture is provided in Appendix B. Each stack comprises four layers of Printed Circuit Board (PCB)s.

The EPS stack includes the following layers:

- Layer 1 – Voltage regulators
- Layer 2 – MCU and battery charger
- Layer 3 – USB-C Power Delivery converter
- Layer 4 – USB-C Power Delivery input and to MPB converter

The USB-C Power Delivery converter on Layer 3 falls outside the scope of this thesis as it is not an essential part of the EPS and is therefore not discussed further. The stack was designed such that the third layer is completely optional and could be added if necessary. The remaining layers are described in detail in the following subsections.

The battery stacks are composed of the following layers:

- Layer 1 – Battery balancing and protection circuitry
- Layer 2 – Voltage subtractors and measurement board
- Layer 3 – Symmetry layer for structural and routing balance
- Layer 4 – Temperature sensor Analog-to-Digital Converter (ADC) and fuse

These layers are described in more detail in Subsection 5.5. Additionally, since the pinouts and exact physical dimensions of the required connectors were not predefined, various connector types and configurations had to be researched. This included selecting suitable connectors and pinout arrangements for the following interfaces: the EPS to main stack, the EPS internal bus, the EPS to battery pack, and the internal bus of the battery pack. All of the electronics designs were done using the program KiCAD 7.0. Schematics of the created designs can be found in Appendix D.

5.3 Connectors

5.3.1 EPS to main stack connector

This interface connects the EPS and battery pack to the rover's main electronics stack. Various options were considered, with Samtec's rugged power connectors, particularly the EXTreme LPHPower series, emerging as a promising candidate due to their low profile,

high pin count, and 30 A current rating per contact line [13]. However, none of the evaluated options provided a sufficient number of power lines to support all required voltages (3.3 V, 5 V, 12 V, and the MPB). Other connectors that did meet the technical requirements were either physically too large or prohibitively expensive.

As a result, a simpler and more accessible solution was chosen: the Peripheral Component Interconnect Express (PCIe) x1 connector. This connector supports up to 2.2 A per pin and includes a total of 64 pins, allowing for flexible allocation of power and signal lines to meet system needs [14]. A custom pinout was created to accommodate all necessary voltage rails and communication lines, while retaining the option to reconfigure certain pins for differential signaling in future development stages. At the time of writing, the system communicates with the EPS via the SPI protocol, with room in place to transition to CAN bus communication in a later phase. The finalized pinout is presented in Appendix Table 2.

5.3.2 EPS internal bus

The EPS internal bus connects all the boards within the EPS stack. The author determined that it would be appropriate to divide the bus into two separate mezzanine board-to-board connectors: one for power and one for internal signals. The signal connector transmits the main bus and internal SPI signals, along with the USB-C CC pins from Layer 3 of the PCB and two analog signals from the voltage regulators on Layers 3 and 4, intended for current measurement by the ADC on Layer 1. The power connector, on the other hand, carries the MPB line, the 24 V input from USB-C for charging, the USB-C output for payloads, and the temperature sensor output lines from Layers 3 and 4.

As the team had already standardized on 2 mm pitch connectors for the main bus, the author chose to adhere to this convention and selected compatible connectors. Ultimately, Samtec's TW and CLT series were chosen as the male and female counterparts of the internal bus connectors. Pass-through connectors were intentionally avoided, as they would complicate disassembly of the stack [15, 16]. Furthermore, opting for a configuration in which only one PCB hosts the male connector while all others use female connectors, rather than having every board equipped with both, was considered to maintain the modularity of the EPS stack.

The pinouts of both connectors are presented in Appendix Tables 3 and 4.

5.3.3 EPS to battery pack connector

The connector between the EPS and the battery pack had to support hot-swapping to allow users to replace batteries easily. Several options were considered, including standard 90-degree pin headers, implementing the entire interface as a single PCB layer, and using spring-loaded pogo pins. Due to their compact size, high advertised mating cycle rating (up

to 100,000 cycles), high current handling capability, and prior experience during debugging on the ESTCube-2 project, the author selected pogo pins for the EPS-to-battery pack connection [17]. The specific components chosen were the Mill-Max 854-22-020-20-001101 pogo pin as the male counterpart and the 856-10-020-20-001000 as the matching right-angle pad [18, 19].

Building on prior research by A. Kütt, the ADC128S102 was identified as the most suitable ADC for the EPS [20, 21]. The final connector's pinout includes the protected battery positive and negative contacts. In addition, a single SPI communication line with two chip select signals and a hot-plug detection pin were incorporated to support communication with the two onboard ADCs, one for temperature monitoring and the other for cell voltage measurement.

The final pinout of this connector is provided in Appendix Table 5.

5.3.4 Battery pack internal bus

The internal bus connector for the battery pack was selected from the same series used for the EPS and main stack, primarily due to its high current rating and its ability to accommodate all necessary signals for communication with the ADCs, as well as other essential signals. The pinout includes connections for battery power, individual cell voltage sensing for the measurement layer, further detailed in Section 5.5.1, and pins for cell temperature monitoring.

The complete internal bus pinout is provided in Appendix Table 6.

5.4 Middle stack

The middle stack is the core of the EPS with the controlling MCU, battery chargers, hot-plug detection, and voltage regulators for powering the entire rover. Due to the usage of the right-angle PCIe X1 for connection to the main stack, the middle stack's first layer was raised by 6.7 mm compared to the rest of the stack and battery packs [14].

5.4.1 Layer 1 - Voltage regulators

To meet the requirement of delivering at least 5 A of current with high efficiency, a survey of commercially available voltage regulator ICs was conducted. Based on this investigation, the author designed and assembled breakout boards for three candidate ICs: the LM61495, TPS56A37, and LT8643SIV [22, 23, 24]. The LM61495 and TPS56A37 were selected for their high current handling capabilities, which provided a comfortable safety margin. The LT8643SIV was included due to its advertised efficiency of up to 95%, its wide operating temperature range, and its capacity to supply up to 6 A of current.

Following the fabrication and testing of the breakout boards, all three regulators were verified to operate correctly. Among them, the TPS56A37 demonstrated the highest overall

efficiency during evaluation and featured a relatively compact footprint, making it the most suitable choice for use in the EPS. This layer also integrates an ADC for real-time monitoring of output voltages, currents, and temperature of the regulators.

Based on the results of this component evaluation, the bottom-most layer of the EPS stack was developed. Renders of this voltage regulation board are shown in Figure 3.

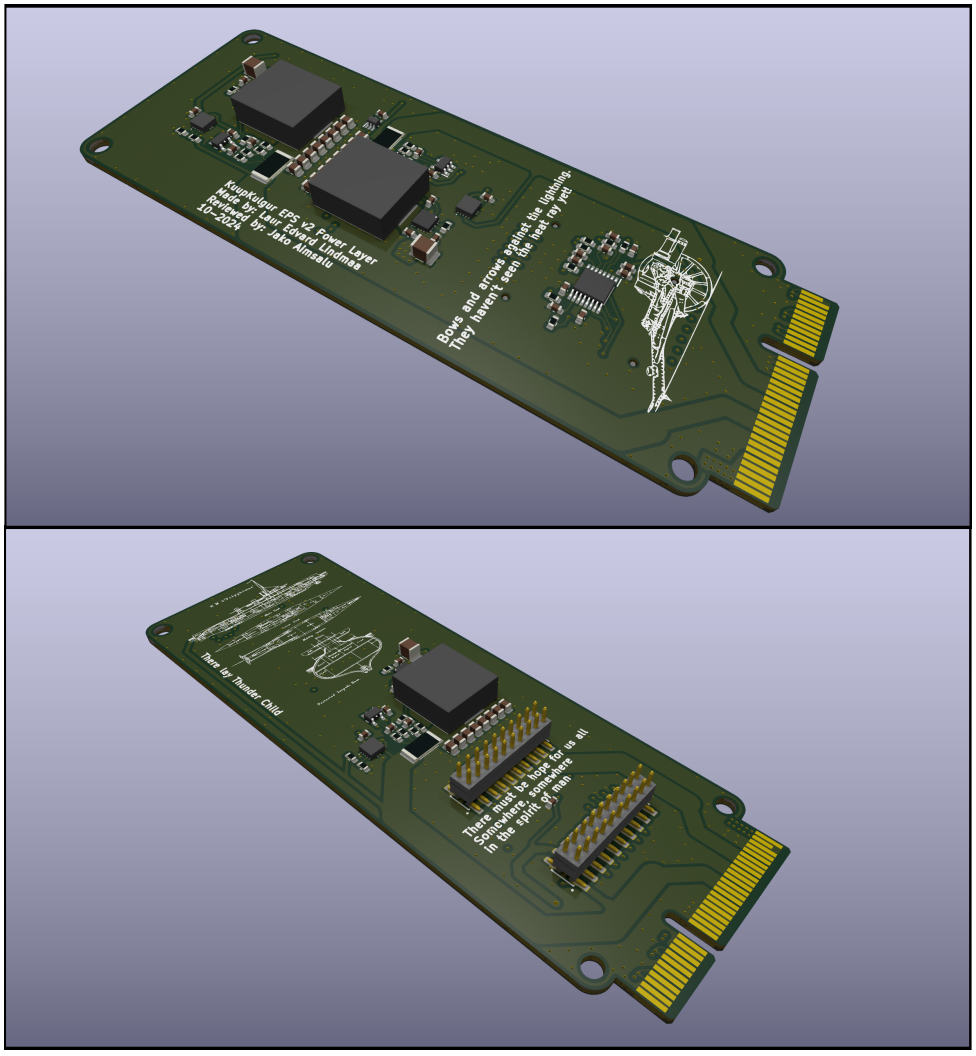


Figure 3: Renders of the EPS-v2 voltage regulator layer

5.4.2 Layer 2 - The MCU and charger

The second layer of the EPS stack contains the MCU responsible for managing both the EPS and battery stacks, while also supplying housekeeping data to the main stack for further processing and analysis. The ATSAMV71Q21B was selected as the MCU, leveraging its prior use as the rover's On-Board Computer (OBC), which ensured compatibility and allowed for design reuse [25]. The MCU offers a sufficient number of General-purpose input/output (GPIO) pins and includes two SPI peripherals that can be independently configured as master and slave. This configuration enables the MCU to simultaneously

communicate with peripheral devices and receive commands from the main bus without requiring mode switching, thereby minimizing communication interruptions and avoiding potential crosstalk with the main stack. To support data logging and diagnostics, an SD card slot was integrated into the board and connected to the MCU via a 4-bit High-speed Multimedia Card Interface (HSMCI). In addition, several auxiliary Input/Output lines were brought out to aid in debugging. Due to the high number of peripheral ICs connected to the MCU, a 3-to-8 multiplexer based on the SN74LVC138ARGYR was also added to simplify signal routing and expand control capability [26].

Aside from its control functionality, this layer also implements the core battery management system. It includes a dedicated charger for each battery pack and incorporates PowerPath circuitry to safely interconnect the packs [27]. This design prevents short circuits in cases where significant voltage differences exist between the packs and provides redundancy in the event of a charger failure. The PowerPath circuitry also manages the transition between battery output and USB-C input, prioritizing power delivery from an external USB-C wall adapter when available during charging operations.

The charging system is built around the BQ24650 integrated circuit, configured to charge the battery packs to a maximum of 20.8 V at 1 A [28]. This voltage level is intentionally set slightly below the nominal 21 V (corresponding to 4.2 V per cell) to enhance battery lifespan during testing. Charging output currents are monitored by the ATSAMV71 MCU using current sense amplifiers based on the INA180, and the MCU is also capable of reading charging status and battery temperatures [29]. This layer includes the physical interfaces to both battery packs. Renders of the designed board are shown in Figure 4.

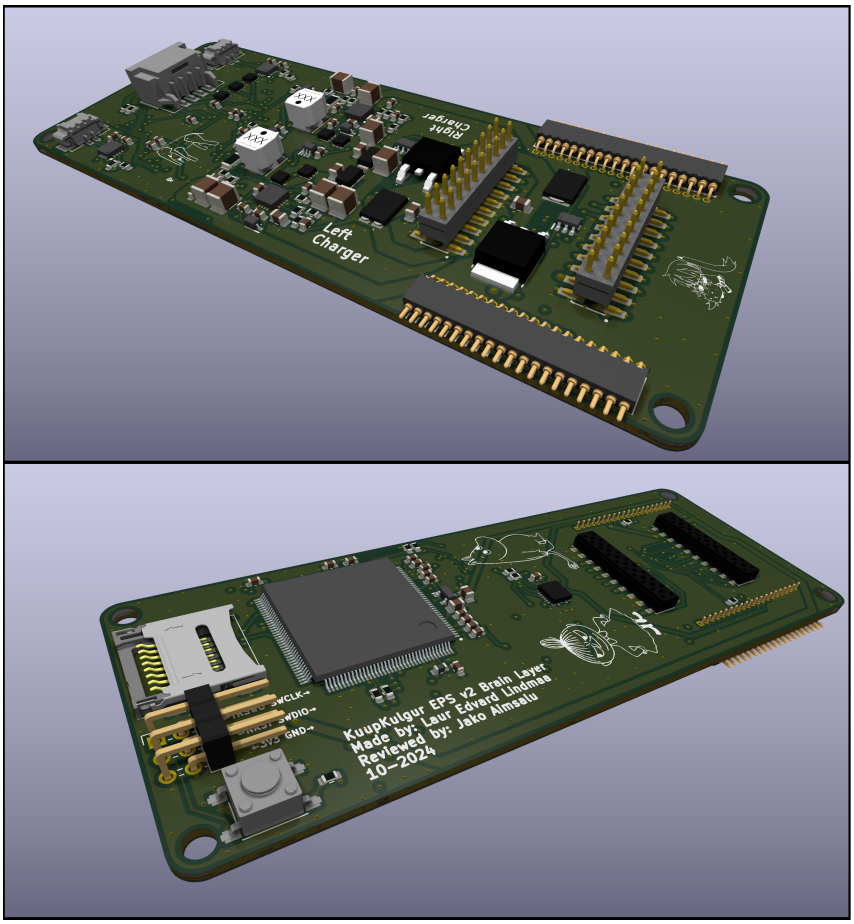


Figure 4: Renders of the EPS-v2 MCU and charger layer

5.4.3 Layer 4 - USB-C Power Delivery input and 24 V converter

The fourth layer of the stack contains a USB-C Power Delivery input/sink and a 24 V converter. The USB-C circuitry is based on the STUSB4500 IC, which is configured to request the highest voltage (up to 20 V) at the highest possible current level according to the Power Delivery 2.0 standard while being interoperable with rev 3.0 [30]. Power from there is sent to the 24 V regulator, which increases whatever voltage comes from the USB-C to 24 V so the battery charging circuit, described in Section 5.4.2, could charge the batteries. One of the limitations of such a system is that because the input voltage can vary a lot, the currents can exceed the USB-C standard at low voltages and possibly not work with chargers that do not provide enough power. A render of layer 4 of the stack is presented in Figure 5.

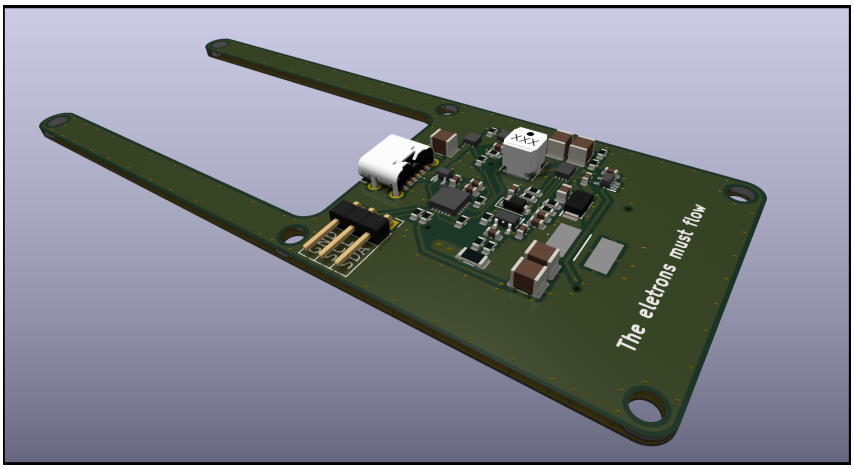


Figure 5: Render of the EPS-v2 USB-C Power Delivery input layer

5.5 Battery stack

The team decided to continue with the earlier approach of using five lithium-ion cells of the type Murata US18650VTC6 connected in series [31]. This setup was considered feasible based on the size constraints, with a backup plan of using four cells in series if five did not fit as expected. The five-cell configuration was preferred, as it had already been used successfully in the EPS-v1. The cells had to be arranged in a way that met the size requirements of the upcoming rover while remaining modular and convenient for debugging and use by other developers. The battery pack was designed so that it would only connect to the internal battery bus when the entire EPS stack was properly assembled. This connection was ensured through a pin header and socket located at the narrower ends of layers 1 and 4.

5.5.1 Layer 1 - Cells and balancing

The first layer of the battery stack includes the connections for the lithium-ion cells and the balancing circuitry. This circuit is based on the BQ7791504PW IC, which had also been used in EPS version one for both cell protection and balancing [32]. In this iteration, the author removed the overcurrent protection functionality and increased the balancing current from 17 mA to 50 mA to maintain more consistent cell voltages during rover operation. Another correction made in this revision was fixing a previous configuration error: the balancer IC had been incorrectly set to handle three cells instead of five. This was resolved by changing the Cell in-series configuration input pin connection from –BATT to a floating configuration. Additionally, the layer includes three 33 kΩ / 4090 K Negative Temperature Coefficient (NTC) thermistors, positioned to monitor cells 1, 3, and 5 [33]. The cells are designed to be spot-welded onto nickel strips, which are then soldered onto the PCB. To secure the cells within the stack, custom cell holders were designed and 3D printed by the team's mechanical lead. A render of this layer is provided in Figure 6.

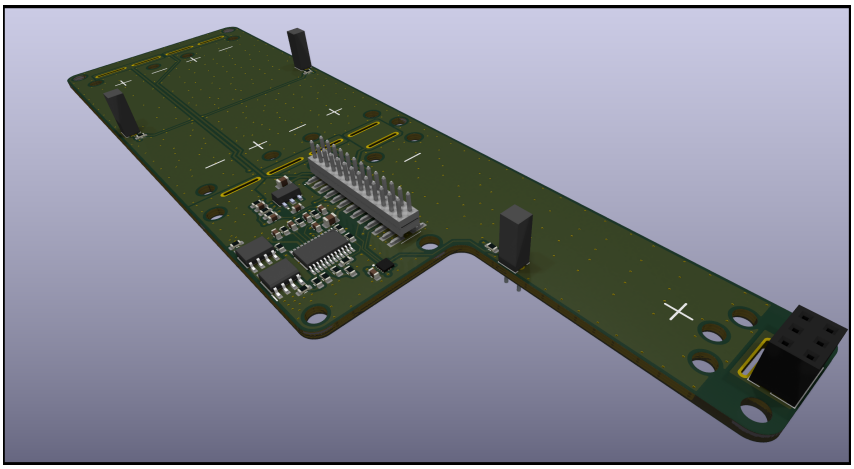


Figure 6: Render of the balancing layer of the battery stack

5.5.2 Layers 2 and 3 - Battery monitoring and symmetry

The second layer of the battery stack contains the measurement circuitry for the individual cell voltages. This layer is built around protected voltage subtractor circuits whose outputs are fed into the ADC. These subtractors are necessary because the battery stack outputs cumulative voltages, where cell 0 marks the unprotected ground: $V_{Cell0} = 0$, $V_{Cell1\_actual} = V_{Cell1\_actual} - V_{Cell0}$, $V_{Cell2\_actual} = V_{Cell2} - V_{Cell1\_actual} - V_{Cell0}$, and so on, which exceed the safe input range of the ADC starting already from the second cell. To extract the individual voltages, dedicated subtractor circuits were used.

Voltage dividers were also considered but ultimately rejected. To match the low input bias current of the OPA4991 operational amplifiers (typically 10 pA) and maintain low current draw, the divider resistors would have needed to be very large, which would have introduced excessive noise. The subtractors, built using OPA4991 operational amplifiers in differential configuration, offered better performance and lower power consumption. Their inputs are protected by Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET)s that only allow voltage through when the battery pack is fully assembled. This avoids damage to the operational amplifiers, which cannot tolerate input voltages more than 0.5 V above their supply voltage [34].

The subtractor outputs pass through low-pass filters with a 150 kHz cutoff, chosen based on the ADC's 1 Msps sampling rate and the use of six measurement channels. Following the filters, Zener diodes clamp the analog lines to a maximum of 5.1 V to protect the ADC and any downstream devices connected to the communication lines.

The author made this design a four-layer PCB because the board size constraints were very limiting compared to the number of components necessary for the required functionality. Renders of the final design are shown in Figure 7.

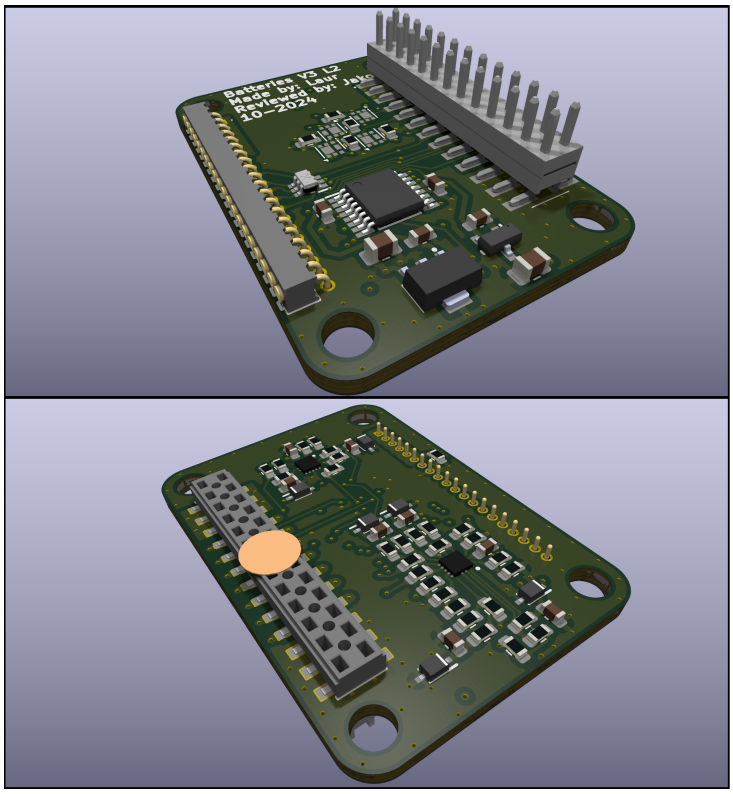


Figure 7: Render of the battery monitoring layer of the battery stack

The third layer of the battery stack was added to preserve symmetry, allowing the same board layout to be used on both the left and right sides of the EPS. Electrically, this PCB only contains the Electrostatic discharge (ESD) protection for external communication lines for protection and bus connectors. Render of the symmetry layer can be found in Figure 8 below.

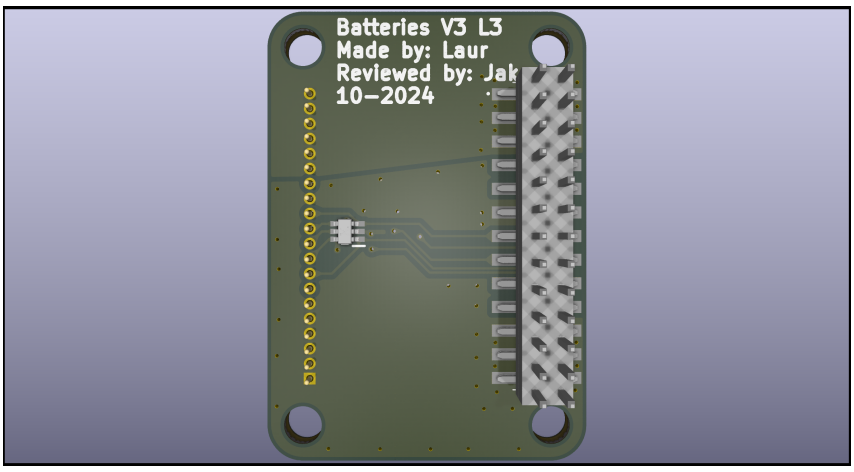


Figure 8: Render of the symmetry layer of the battery stack

5.5.3 Layer 4 - Fuse and temperature monitoring

The final layer of the battery pack stack houses a 10 A fast-blow fuse to protect the rover prototype in the event of an electrical failure. It also includes the same 33 kΩ / 4090 K NTC thermistors used on the first layer, along with an ADC that measures their outputs [33]. When this layer is connected to the first stack, it completes a loop that connects the batteries to the battery bus, thereby enabling the electronics. A render of layer 4 is shown in Figure 9.

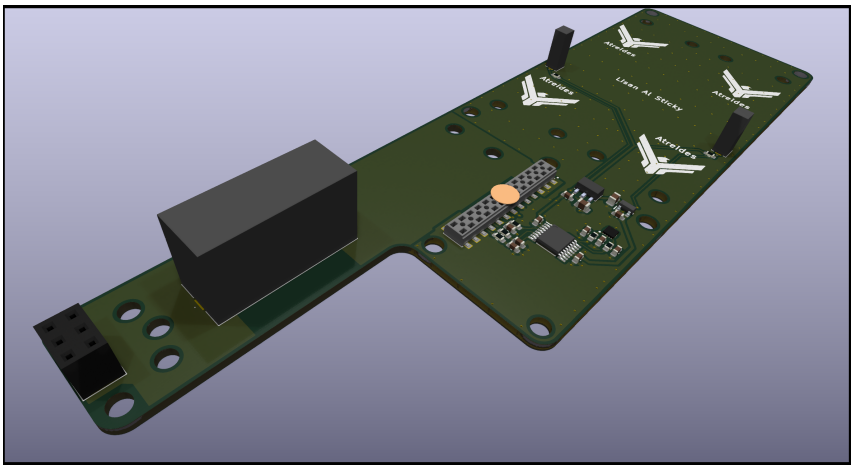


Figure 9: Render of the fuse and temperature monitoring layer of the battery stack

5.6 Assembly

5.6.1 Mechanical considerations

After completing the design and peer review of all the PCBs, they were ordered and assembled in the electronics laboratories at the Tartu Observatory. For testing the EPS and battery stacks together, the author made a 3D-printable underboard which had the same dimensions and screw holes as the planned rover. During the assembly and testing, it was discovered that the Mill-Max pogo pins were unsuitable for use in the originally intended configuration. Specifically, maintaining proper alignment of the pogo pins proved difficult during testing. Another recurring issue during the battery installation process was the misalignment of the pogo pins, which occasionally resulted in electrical shorts. In some instances, the main positive terminal of a battery made unintended contact with an SPI line, despite an intentionally left unconnected pin between the power and data lines for isolation. These shorts led to damage to critical components, including the ATSAMV7 MCU and the ADCs. The pins frequently shifted vertically away from the pads, tended to bend under stress, and were challenging to insert due to the limited space available for initial compression. Examples of mechanical faults are displayed in Figure 10, where the upper image contains pins that have become stuck due to bending, and the bottom shows

vertical bending.

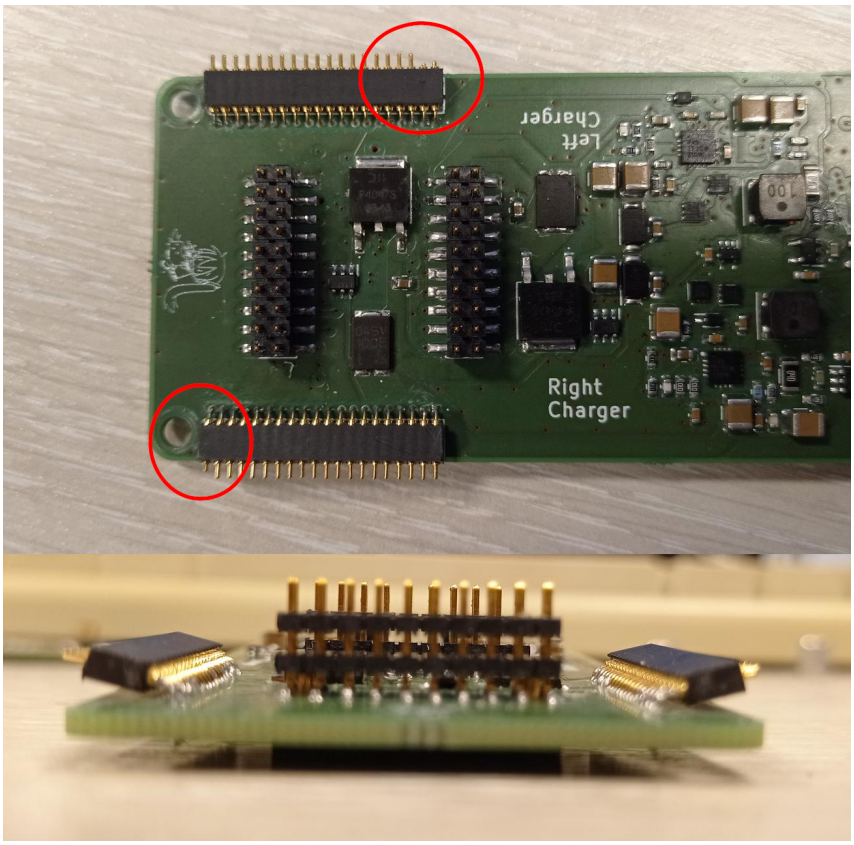


Figure 10: Examples of mechanical failures on the pogo-pin connector, circled in red

To address these issues, the author decided to forgo the hot-plug capability of the battery packs and instead implemented permanent wire bridges between the batteries and the EPS. While this solution significantly improved the reliability and security of the electrical connections, it also eliminated the possibility of swapping batteries without disassembling the entire stack. Following the transition to the permanent soldered connections, which are also shown in the Figure 11, such issues were resolved, and testing of the EPS was able to proceed without further electrical failures.

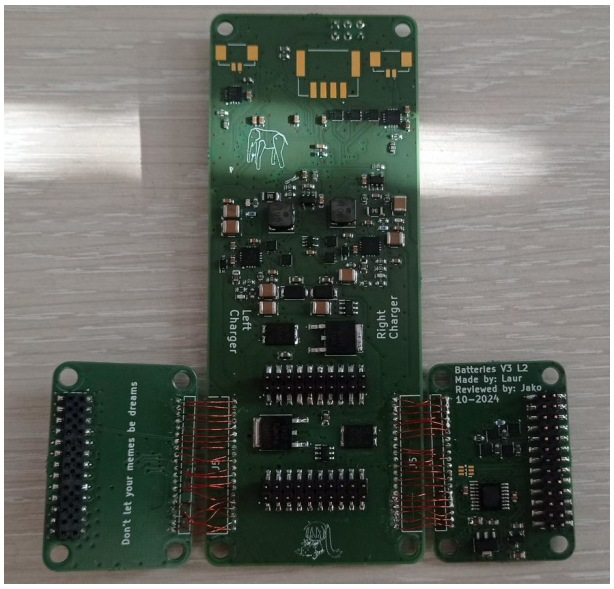


Figure 11: EPS middle stack with soldered permanent wires

5.6.2 Final assembly

The EPS and battery stacks were assembled according to the requirements set by the team. M3 screw holes and standoffs were incorporated into all the boards to securely hold them in place and maintain proper spacing between the layers. One of the challenges encountered during assembly was that soldering the lithium-ion cells to the first layer caused parts of the cells to extrude from the board, exposing areas with voltage potential. To address this, Kapton tape was applied to the opposite side of the board, covering the exposed metal contacts to prevent any short circuits. The fully assembled EPS and battery stacks are shown in Figure 12. Once the stack was complete, testing of the electronics could begin.

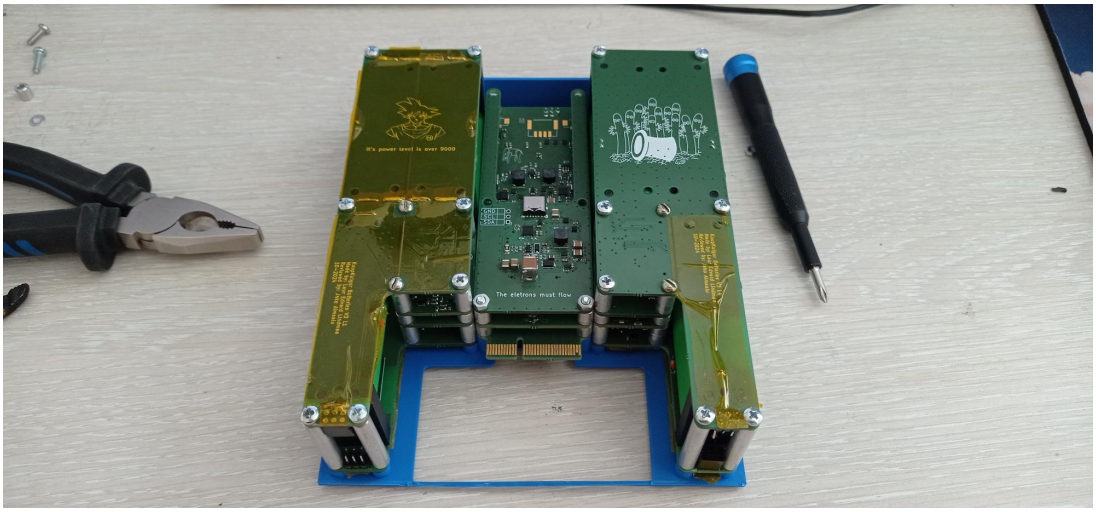


Figure 12: Fully assembled EPS and battery stack

5.7 Laboratory testing and analysis

To make sure the newly developed design could be used on the next revision of the KuupKulgur prototype, all of the modules had to be tested. For that, the author created the following test campaign plan.

- Test the functionality of voltage regulators
- Measure the battery pack's idle lifespan
- Perform a complete functional test

5.7.1 Voltage regulators

To test the voltage regulators, the author made a breakout board, shown in Figure 13, that connects to the EPS and brings out all of the power lanes, making it easy to connect them with crocodile clips and then to the current sink.

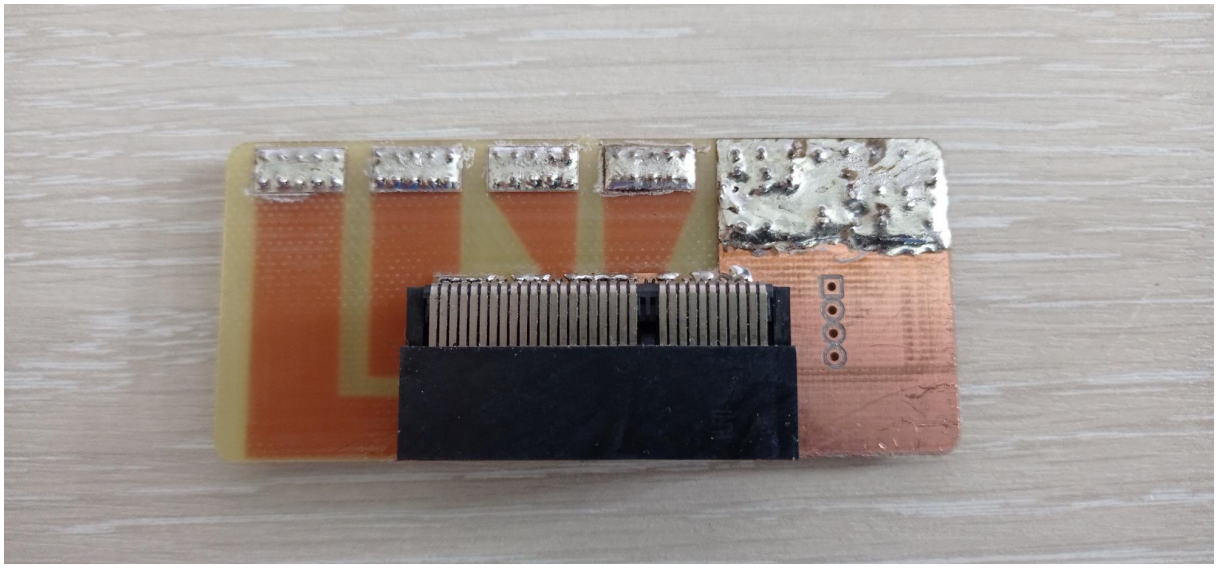


Figure 13: EPS breakout for current sinks

The voltage regulators were tested by supplying either 18 V or 21 V to the main power bus to simulate the nominal battery voltage. The current draw of each regulator was incrementally increased in 0.1 A steps until the target load of 5 A was reached. A schematic of the test setup is presented in Figure 14. Temperature measurements were conducted using an Infiray C200+ thermal camera [35]. Power was supplied using a Rigol DP823A programmable power supply [36]. Two UT58A multimeters were used during testing: one configured to the 200 V mode to monitor the voltage on the main power bus, and the other set to 20 V mode to measure the output voltage of the regulators directly [37].

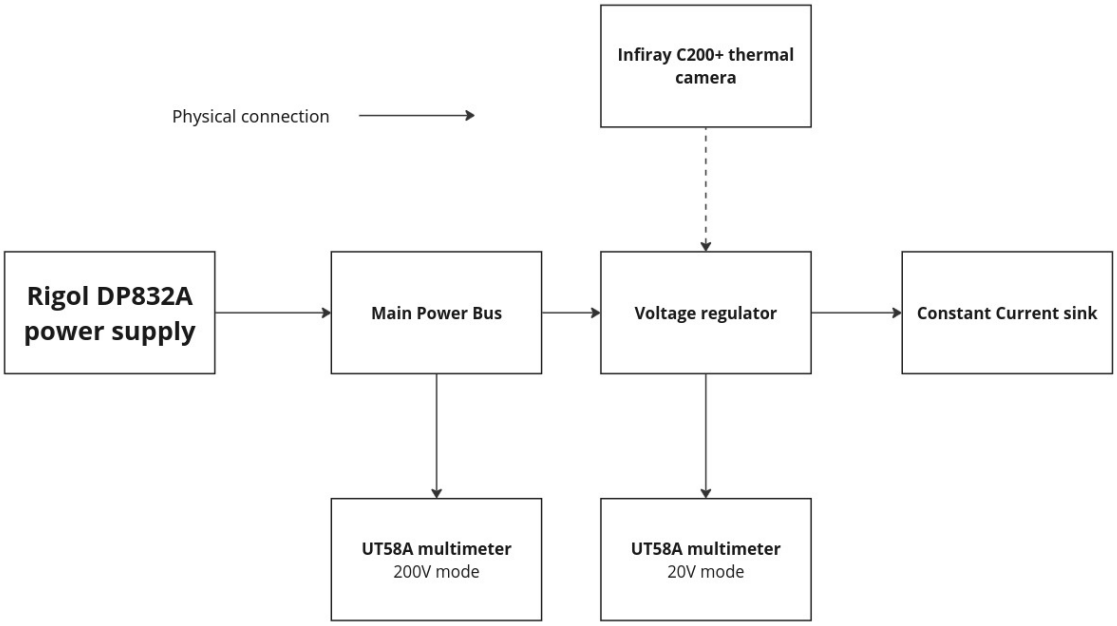


Figure 14: Voltage regulator test setup

The test campaign demonstrated that all regulators maintained output voltages within ±10% of their nominal values and remained below the 80 °C temperature threshold. The maximum recorded temperatures for the 12 V, 5 V, and 3.3 V regulators were 75.60 °C, 55.6 °C, and 59.7 °C, respectively. The corresponding mean efficiencies were 95.52%, 92.00%, and 87.49%. The results of the efficiency test are shown in Figure 15. Although the 3.3 V regulator exhibited comparatively lower efficiency, no changes were made, as the actual current draw on that rail was negligible in the current prototype. Furthermore, even at maximum load, the 3.3 V regulator did not exhibit significant thermal buildup. The thermal imaging results are provided in Appendix E.

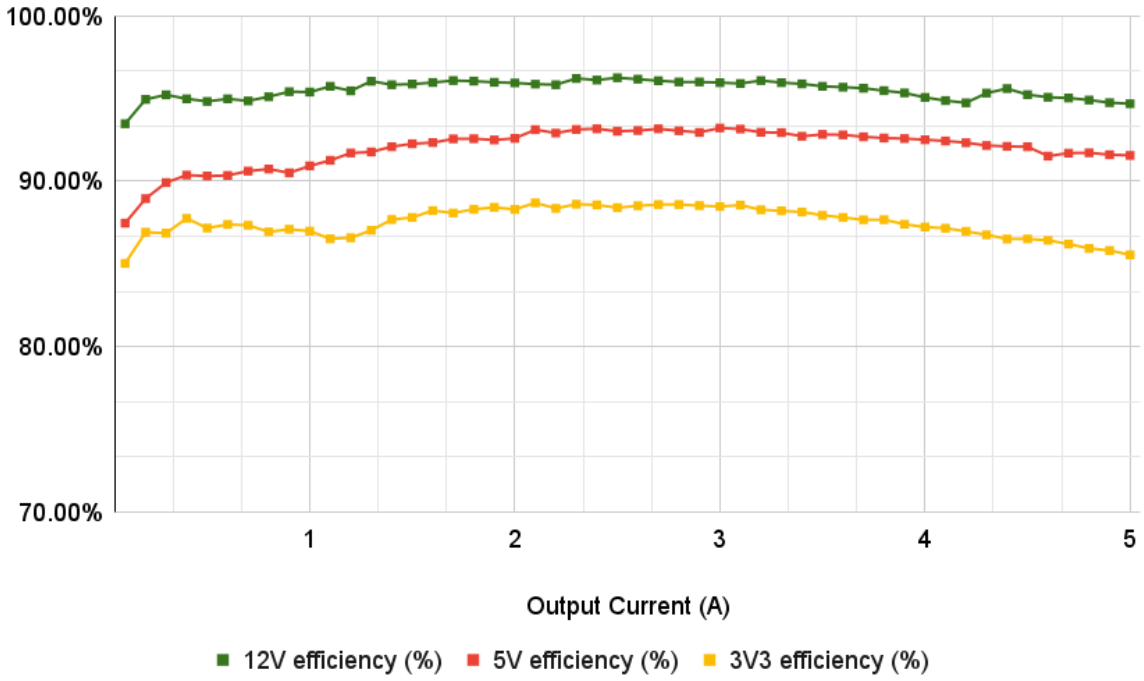


Figure 15: EPS-v2 voltage regulator efficiencies at different output currents

5.7.2 Battery pack idle test

The second test performed on the stack was the battery pack idle test, during which the battery pack was detached from the EPS and placed into its active state. Over the course of a day, both the cell voltages and the current draw were recorded. From the collected data, it was possible to estimate the idle lifespan of the battery pack, for example, how long the stack can remain enabled in storage without EPS connection. Voltage was measured across the battery pack's + and – output contacts, while current was measured by placing a multimeter between the end connectors of layer 1 and layer 4. This setup also acted as an enabling switch. The battery voltage levels over time are plotted in Figure 16.

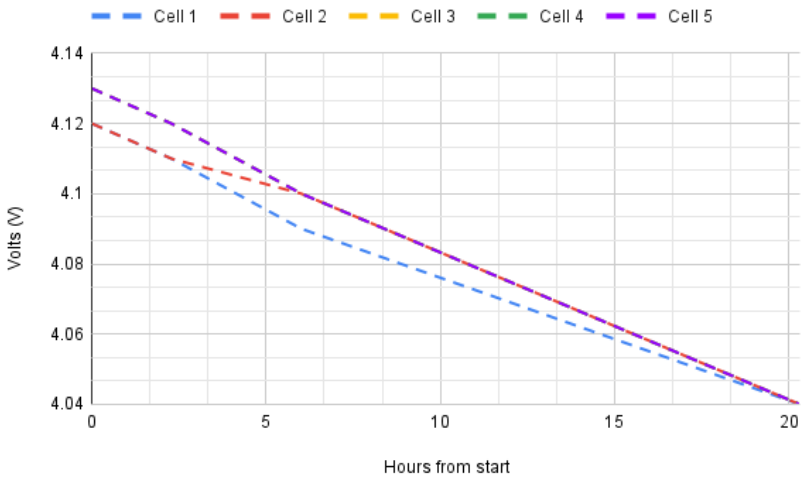


Figure 16: Battery pack cell voltages over time during idle test

The results show that the battery pack's total voltage drops at an average rate of 0.0221 V per hour. The current draw remained constant at 10.8 mA throughout the measurement period. According to the cell datasheet, the full charge voltage is 4.2 V, and the minimum recommended cutoff is 2.5 V [31]. However, since the voltage begins to drop steeply around 3 V, a cutoff at 3 V was chosen to increase cell longevity. Based on these values, it was determined that the battery pack could remain enabled for approximately 11 days, discharging about 2978 mAh over that period. The current draw remains constant because, with the exception of the balancer, all onboard electronics are powered through Low-dropout regulators. These components supply the ICs with a constant, reduced voltage by dropping the excess input voltage and dissipating it as heat.

5.7.3 Final functionality test

The final functionality test was performed with the entire EPS and battery stack fully assembled. The author conducted this test to verify that all modules worked together. First, a USB-C cable was connected to check whether the highest possible voltage (20 V) would be successfully negotiated. After confirming this, the output of the 24 V regulator was measured and found to be 23.68 V. Because this was significantly lower than expected, the author investigated further using an Infiray C200+ thermal camera to measure the board's temperature and cross-referenced both the schematic and the regulator's datasheet [35]. This analysis revealed that the regulator was operating at 78 °C and was realistically capable of supplying only 3 A, close to the current already drawn by the charging circuits (2 A), not including the rest of the electronics stack. To confirm that the charging circuits functioned correctly, the voltage drop across their shunt resistors was measured. A drop of 40 mV was observed, corresponding to a 1 A current given the 40 mΩ shunt resistance. Next, the voltage regulators were verified under 0 A and 5 A load conditions to ensure they

behaved consistently with the previous results described in Section 5.7.1. As all modules operated as expected, the test concluded that the design was overall successful, with only minor errata to be addressed in future revisions.

It was not possible to test the EPS-v2 and battery stack inside the rover prototype, as the rest of the electronics required for its operation were still in development.

6 EPS-v1.1

As one of the requirements of this thesis was to apply lessons learned from designing the EPS-v2 to improve the currently used rover prototype, the author took the EPS-v1 design and replaced its electronic modules with more compact variants based on the same ICs selected for EPS-v2. The complete architecture of EPS-v1 can be found in Appendix B. Render of the designed board can be seen in Figure 17.

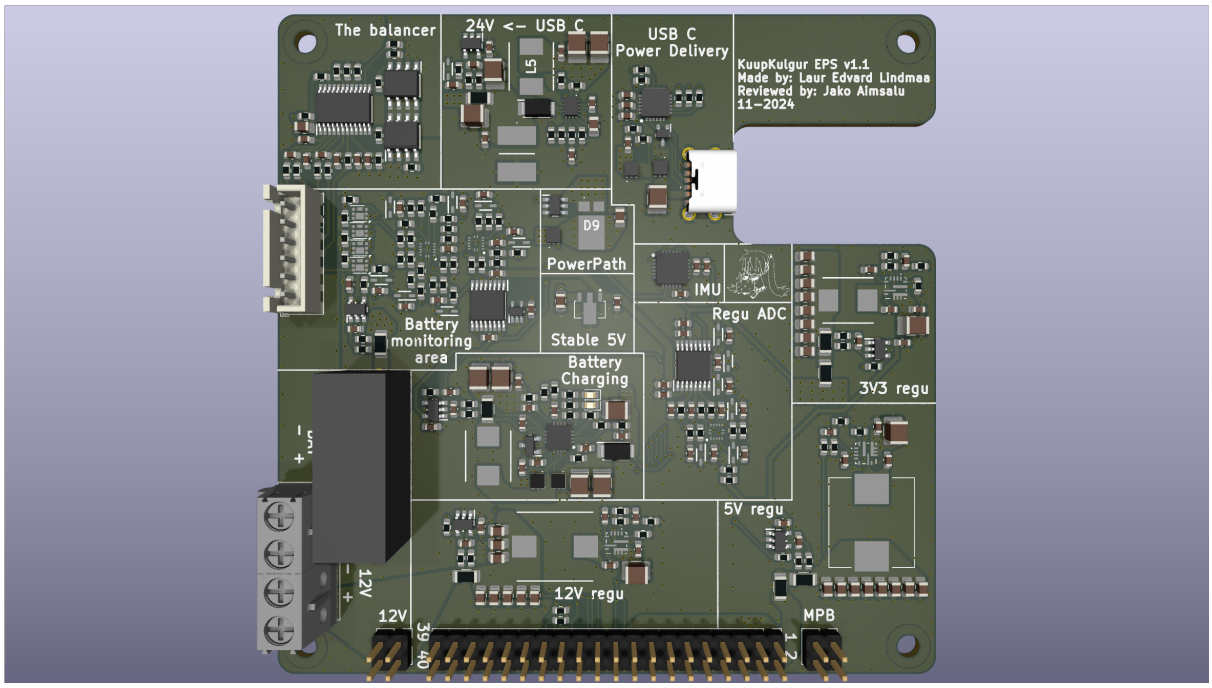


Figure 17: Render of the updated version of the EPS

6.1 Laboratory testing and analysis

Similarly to EPS-v2, version 1.1 of the EPS had to be tested before it could be considered ready for use in the rover. Before the rover could be operated using the EPS, the following modules required verification:

- USB-C Power Delivery input
- 24 V regulator

- Battery charger and balancer
- PowerPath
- 3.3 V, 5 V, and 12 V regulators
- IMU

In EPS-v1.1, the inductor for the 24 V regulator was replaced with one rated for higher current (5.5 A). As in EPS-v1, the IMU is integrated into the EPS, as it is not present elsewhere in the rover's electronics stack. The testing methodology for the modules was the same as that used for EPS-v2, with the exception of the IMU, which required direct connection to verify functionality.

Each regulator was able to successfully supply up to 5 A of current. The measurements were conducted with an input voltage of 24 V. The results for both EPS-v1 and EPS-v1.1 are shown in Figure 18. From these, the efficiency improvements in version 1.1 are clearly visible: the 12 V and 5 V regulators consistently maintained efficiencies above 90%, while the 3.3 V regulator remained mostly between 87.5% and 90%. In contrast, the regulators in version 1 dropped below 90% even at lower currents, and below 80% when the output exceeded 2.5 A. The original board could not reach higher current levels due to thermal shutdowns of the voltage regulators. The thermal imaging results are provided in Appendix E. The exact thermal data for the EPS-v1 is missing due to the thermal camera being unavailable at that time.

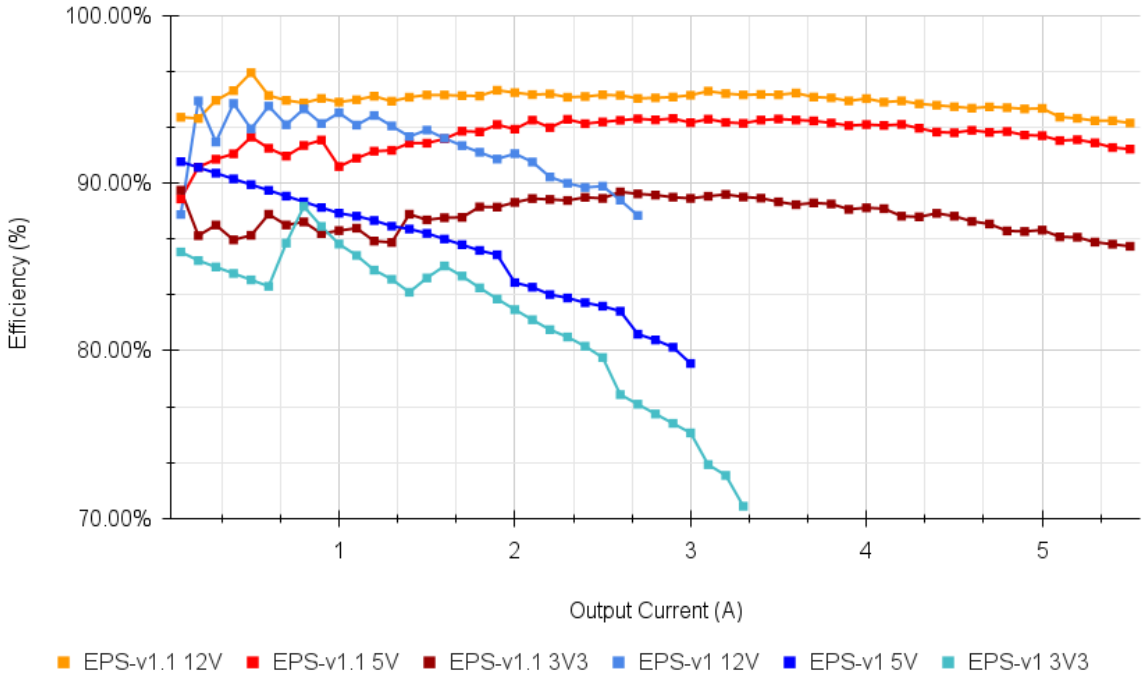


Figure 18: EPS version 1 and 1.1 efficiencies at different output currents

7 Full stack testing

Full-stack testing of EPS-v1.1 involved driving the rover around the Tartu Observatory's lunar analogue facility and in Tõravere, both with and without a mock payload acting as a current sink. The purpose of the test was to demonstrate that the rover could be reliably operated while collecting data under varying load conditions.

The author first performed the test drives using the EPS-v1 system to collect baseline data for later comparison. In total, four test drives were conducted: two in the Lunar Analog Facility of Tartu Observatory using LiDAR, and two outdoors without it. Each test began when the EPS indicated that the batteries were fully charged and ended when any cell voltage dropped to 3.4 V. The cells were not discharged down to the 3.0 V cutoff in order to prolong battery lifespan and because performance could be reasonably estimated by comparing the measured data to the battery datasheet.

Similar to EPS-v1.1, the EPS-v1 test was run in two modes: with LiDAR enabled and in free-roam mode without it. With LiDAR, runtimes were 1201 and 1212 seconds, corresponding to useful battery capacities of 16.69 Wh and 17.09 Wh. In free-roam mode, the rover lasted 2453 and 2744 seconds, delivering 19.84 Wh and 21.07 Wh of usable energy, respectively. From these figures, the average power consumption was calculated as 50.40 W with LiDAR and 28.38 W without.

The same tests were repeated with EPS-v1.1 under identical conditions. With LiDAR enabled, runtimes increased significantly to 2154 and 2248 seconds, yielding 30.26 Wh and 32.99 Wh of usable capacity. In free-roam mode, the rover ran for 4100 and 4506 seconds, using 33.99 Wh and 38.18 Wh, respectively. Corresponding average power consumption values were slightly higher than with EPS-v1: 51.70 W with LiDAR and 30.17 W without.

Additional data was collected during the test drives, but it was not possible to accurately determine the driven distance due to unreliable encoder data and the fact that LiDAR-based localization was still under development.

7.1 Results

The collected data revealed a significant improvement in the rover's operational lifespan. According to the battery datasheets, the difference in capacity between 3.4 V and 3.0 V is approximately 900 mAh, which corresponds to 3.24 Wh per cell or 16.2 Wh total, assuming a nominal voltage of 3.6 V. The theoretical capacity from 4.2 V to 3.4 V is about 1900 mAh (6.84 Wh per cell or 34.2 Wh total). This suggests that the main advantage of EPS-v1.1 over EPS-v1 is its ability to utilize the full battery capacity range, something the original version could not achieve. However, what was unexpected was that EPS-v1.1 consumed noticeably more power than its older counterpart, even though the architecture was mostly the same and the voltage regulators were significantly more efficient. An example of the data gathered during a test drive can be seen in Figures 19 and 20. Note

that the current drops on 19 are not due to measurement error, but due to the rover driving around and stopping for some time.

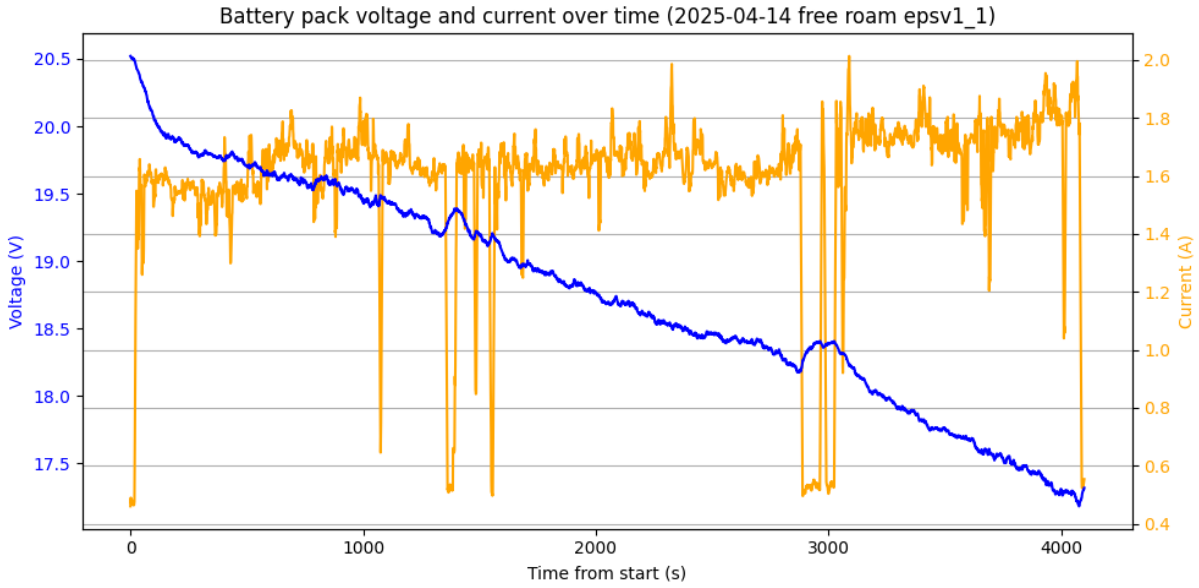


Figure 19: Total output current and MPB voltage during the test

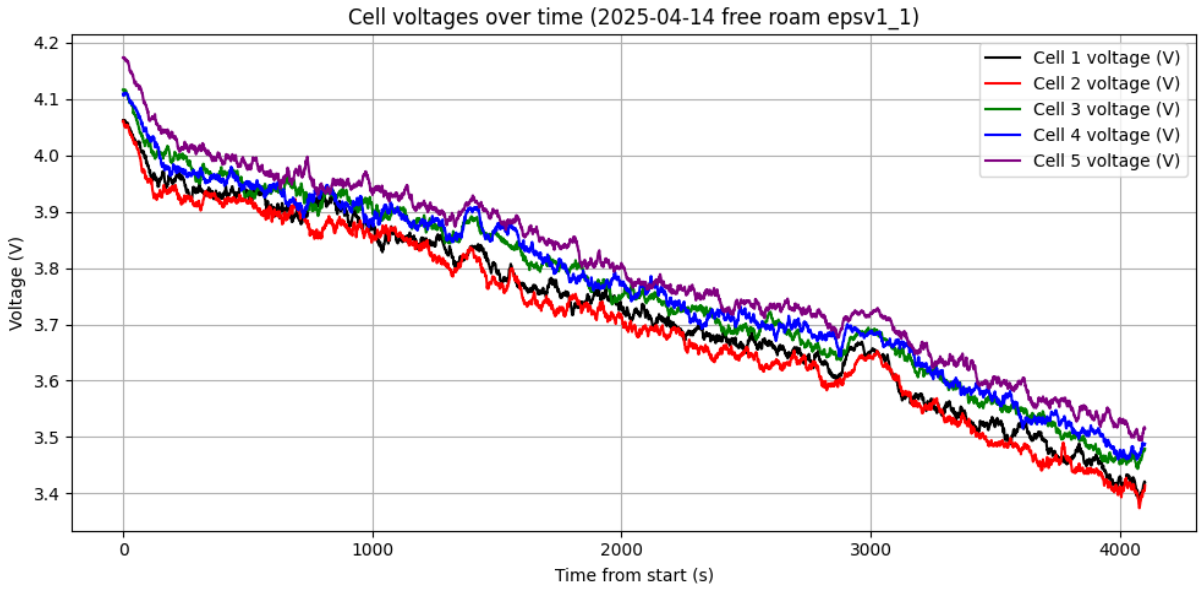


Figure 20: Cell voltages during the test

7.1.1 After-test troubleshooting

As a result, the EPS-v1.1 was further inspected, revealing that the voltage subtractor circuit was generating unexpected heat. As shown in Figure 21, the maximum temperature in that area reached 99.6 °C.

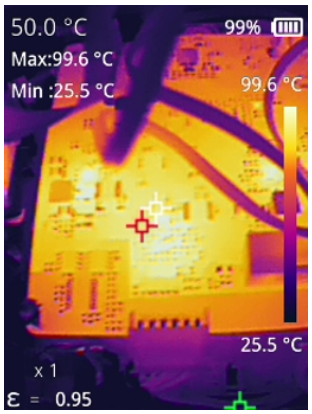


Figure 21: Voltage subtractor generating excessive heat

This prompted the author to revisit the schematic used during development, where a design mistake was discovered in the $cell5 - cell4$ voltage subtractor circuit. Specifically, cell 5 was directly connected to the input of the OPA4991 operational amplifier, rather than to BAT+, which was intended to be disconnected when the rover is powered off. This introduced an edge case where the amplifier input remained connected to the battery while its supply voltage was at 0 V, greatly exceeding the allowable input voltage range and leading to failure of the IC. To avoid ordering and assembling a completely new board, the author implemented a hardware fix by cutting the BAT5 connection to the operational amplifier and rerouting it to BAT+ instead. After addressing the issue, one free-roam test and one LiDAR-enabled test were repeated. The LiDAR test showed no significant change in current consumption, while the non-LiDAR test demonstrated a 5% reduction in current usage compared to the results before the fix. Overall, the rover consumed 49.27 W with LiDAR and 25.58 W without it, representing a reduction of 1.13 W with LiDAR and 2.8 W without it in power consumption compared to version 1 of the EPS. Despite the correction in the voltage subtraction circuit, the operational amplifiers continued to exhibit thermal buildup, reaching temperatures of around 40 °C. An infrared image of the circuit after the fix is shown in Figure 22.

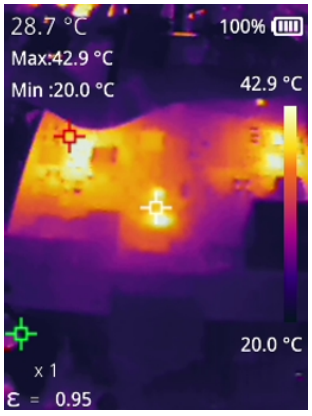


Figure 22: Thermal camera image of the EPS after the aforementioned fix

8 Future work

Some improvements and errata have been identified for future iterations of the EPS. One of the most pressing issues is the excessive heat generated by the voltage subtractor circuit. Despite correcting a schematic error, the component still experiences elevated temperatures during operation. After consulting with the electronics leads of the student satellite project, it was suggested to evaluate the BQ76905 series integrated circuit as a potential solution for cell balancing and monitoring. This IC may offer a more integrated and thermally efficient design. Additionally, the thermal performance of the 24V regulator on the EPS-v2 needs to be investigated, as currently it shows significant heat buildup. Thus, it should be replaced with a more efficient component that can handle the expected power demands without thermal issues.

Another consideration is the mechanical and electrical interface of the battery modules. Since batteries are not expected to be replaced in space, hot-swappability is not a requirement for the final space-ready version. However, it remains a useful feature for prototype testing to reduce downtime while waiting for batteries to charge. The current pogo pin solution has reliability issues, and a more robust alternative should be pursued. One possible approach is to develop a breakout board into which both the batteries and the EPS can be connected. If designed appropriately, this board could also replace the PCIe connector and be extended to serve the entire electronics stack.

In addition, future revisions of the EPS should implement CAN communication using the existing pins currently used for SPI communication with the main stack. CAN offers a more robust and fault-tolerant alternative to point-to-point interfaces like SPI, and its use as a shared bus would likely reduce wiring complexity and free up pins on the OBC, contributing to a cleaner and more scalable system architecture.

Finally, while not within the scope of this thesis, any future EPS revisions intended for space must undergo environmental testing. This includes thermal-vacuum testing to simulate the temperature extremes and vacuum conditions of space, as well as radiation testing to verify the durability of the components under space radiation levels.

9 Conclusion

The primary objective of this Master's thesis was to develop a new EPS for the next revision of the KuupKulgur lunar rover prototype, while also improving the existing system through targeted debugging and troubleshooting to ensure reliable operation.

The main contributions of this work were:

- The design and implementation of a new EPS that meets the defined requirements
- Selection of a robust interface for both power delivery and communication
- Extension of the operational lifespan of the current rover prototype through improved power efficiency
- Verification and validation of system functionality through extensive testing

All of the functional requirements outlined at the beginning of the project were successfully fulfilled, with the exception of hot-swappability for the new EPS, which was deprioritized as it is not essential for the final space-ready version.

Acknowledgements

The author would like to express his deepest gratitude to his thesis instructors for providing support, guidance, and expertise throughout the entire process.

The author would also like to thank Kristin Kandelin from the Student Satellite Foundation and other KuupKulgur team members for their guidance, encouragement, and for providing ideas to improve the quality of the work.

Additionally, the author acknowledges Terrence Andrew Davis for being a remarkable inspiration with his unique approach to programming and unwavering dedication.

Finally, the author would like to express his appreciation to his family and friends for their support in writing this thesis.

/signed digitally/

References

[1] "Common european research classification scheme (cercs): Teadusvaldkondade ja -erialade klassifikaator." https://wiki.ut.ee/download/attachments/16581162/Common%20European%20Research%20Classification%20Scheme.pdf. Accessed: 2025-05-17.

[2] NASA, "The Artemis Program." https://www.nasa.gov/humans-in-space/artemis/, 2025. Accessed: 2025-05-12.

[3] NASA, "Gateway." https://www.nasa.gov/mission/gateway/, 2025. Accessed: 2025-05-12.

[4] Astrobotic Technology Inc., "Cuberover specifications." https://science.nasa.gov/wp-content/uploads/2023/11/astrobotic-cuberover.pdf, 2023. Accessed: 2025-05-14.

[5] NASA, "Electrical Power Systems for Cubesats." https://ntrs.nasa.gov/api/citations/20180007969/downloads/20180007969.pdf, 2018. Accessed: 2025-05-17.

[6] NASA, "Moon facts." https://science.nasa.gov/moon/facts/, 2025. Accessed: 2025-05-12.

[7] J. S. Halekas, R. P. Lin, and D. L. Mitchell, "Large negative lunar surface potentials in sunlight and shadow," *Geophysical Research Letters*, vol. 32, no. 9, 2005.

[8] NVIDIA, "Jetson Orin Nano Developer Kit." https://www.nvidia.com/en-us/autonomous-machines/embedded-systems/jetson-orin/nano-super-developer-kit/, 2025. Accessed: 2025-05-16.

[9] Gadgetoid, "Raspberry Pi Pinout." https://pinout.xyz/, 2025. Accessed: 2025-05-16.

[10] Texas Instruments, *TPS563300 datasheet*, 2022. Accessed: 2025-05-16.

[11] J. Adams, M. Bhattacharya, Z. Lin, G. Pendleton, and J. Watts, "The ionizing radiation environment on the moon," *Advances in Space Research*, vol. 40, no. 3, pp. 338–341, 2007.

[12] I.-C. Cho, C. M. Tan, N. A. Baruah, A. Shabir, H. T. T. Singh, T.-C. Chao, and C.-H. Chu, "Degradation analysis of commercial off-the-shelf (COTS) electronics system under gamma radiation," *Results in Engineering*, vol. 25, p. 103802, 2025.

[13] Samtec, "Extreme lphpower™ specifications." https://www.samtec.com/rugged-power/power-systems/extreme-lphpower/, 2025. Accessed: 2025-05-16.

[14] Samtec, "Pci Express® edge card sockets." https://www.mouser.ee/datasheet/2/527/pcie-2854633.pdf, 2025. Accessed: 2025-05-16.

[15] Samtec, "Tw-sm 2.00 pitch terminal strip." https://www.samtec.com/products/tw-sm, 2025. Accessed: 2025-05-16.

[16] Samtec, "Clt connector." https://www.samtec.com/products/clt, 2025. Accessed: 2025-05-16.

[17] Mill-Max, "Mill-max spring loaded connectors." https://www.mill-max.com/catalog/download/2018-05%3A018.1M.pdf, 2025. Accessed: 2025-05-16.

[18] Mill-Max, "Mill-max Spring loaded poho pin header specifications." https://www.mill-max.com/products/spring-loaded/pogo-pin-header-strip/854/20-001101/854-22-020-20-001101, 2025. Accessed: 2025-05-16.

[19] Mill-Max, "Mill-Max Mating target pad connector specifications." https://www.mill-max.com/products/mating-target/pad-connector-with-flat-face/856/20-001000/856-10-020-20-001000, 2025. Accessed: 2025-05-16.

[20] A. Kütt, "ADC tarkvara arendamine ja testimine kuupkulguri projekti jaoks." https://digikogu.taltech.ee/et/Item/151a8f92-c39f-430b-bffb-8c4489ce726f, 2024. Accessed: 2025-05-16.

[21] Texas Instruments, *ADC128S102 Datasheet*, 2015. Accessed: 2025-05-16.

[22] Texas Instruments, *LM62460-Q1 Voltage regulator Datasheet*, 2021. Accessed: 2025-05-16.

[23] Texas Instruments, *TPS56A37 Voltage regulator Datasheet*, 2024. Accessed: 2025-05-16.

[24] Analog Devices, *LT8640S Voltage regulator Datasheet*, 2023. Accessed: 2025-05-16.

[25] Microchip, *ATSAMV71Q21B MCU Datasheet*, 2023. Accessed: 2025-05-16.

[26] Texas Instruments, *SN74LVC138A 3-Line to 8-Line Decoder Datasheet*, 2016. Accessed: 2025-05-16.

[27] Linear Technology, *Low Loss PowerPath™ Controller Datasheet*, 2015. Accessed: 2025-05-16.

[28] Texas Instruments, *BQ24650 Stand-Alone Synchronous Buck Battery Charge Controller*, 2020. Accessed: 2025-05-16.

[29] Texas Instruments, *INAx180 current sense amplifier Datasheet*, 2022. Accessed: 2025-05-16.

[30] STMicroelectronics, *STUSB4500 Standalone USB Power Delivery sink controller Datasheet*, 2020. Accessed: 2025-05-16.

[31] Murata Manufacturing Co., Ltd, *US18650VTC6 Cylindrical Type Lithium-Ion Secondary Battery*, 2012. Accessed: 2025-05-16.

[32] Texas Instruments, *BQ77915 Battery Protection and Balancing IC Datasheet*, 2023. Accessed: 2025-05-16.

[33] Vishay BCcomponents, *NTCLE100E3 Thermistor Datasheet*, 2025. Accessed: 2025-05-16.

[34] Texas Instruments, *OPAx991 Rail-to-Rail Operation Amplifier Datasheet*, 2022. Accessed: 2025-05-16.

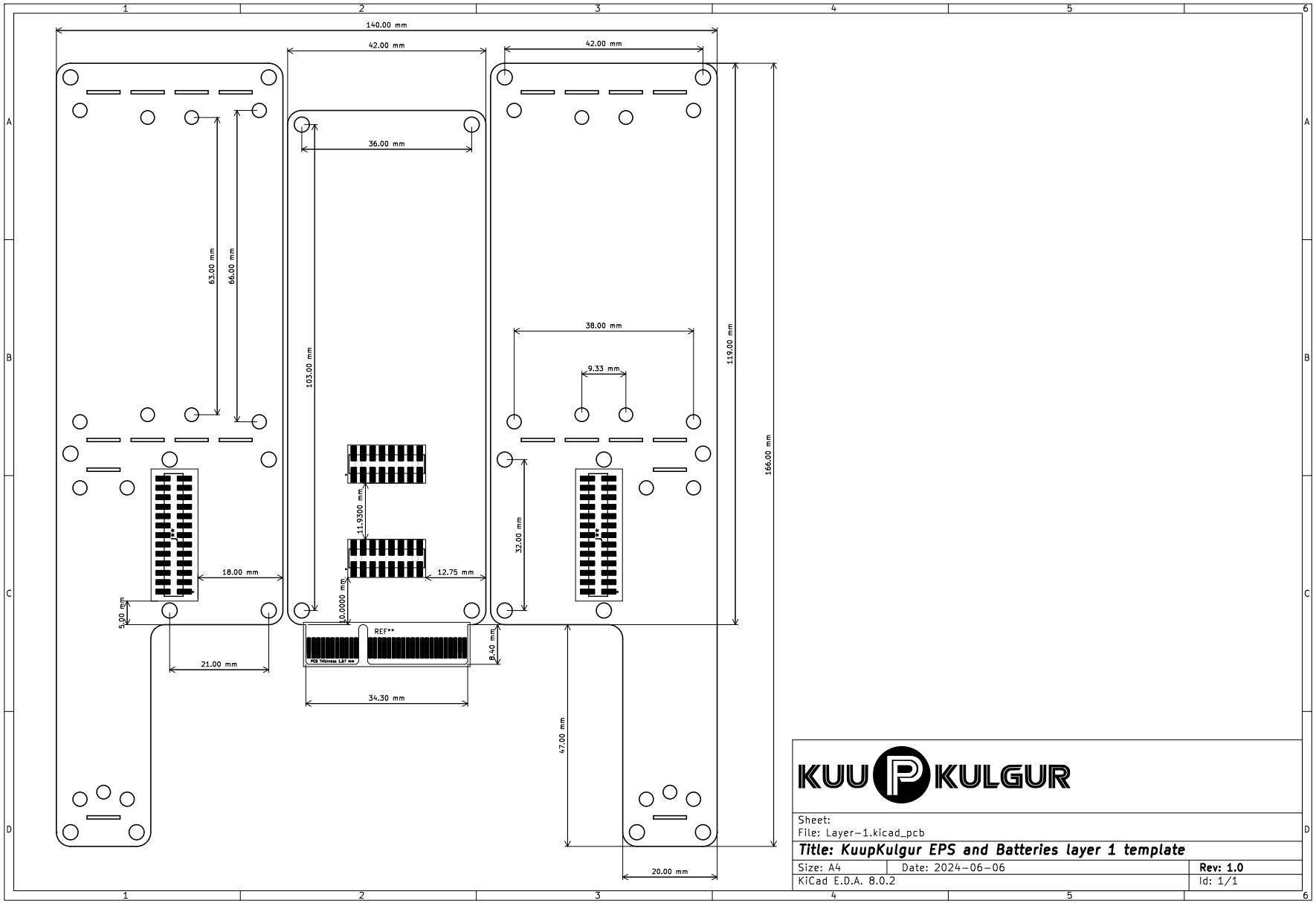
[35] Eleshop B.V., "Infiray C200+ Store Website." `https://eleshop.eu/infiray-c200-plus.html`, 2025. Accessed: 2025-05-17.

[36] Rigol Technologies INC., "DP800 Series Specifications." `https://www.rigolna.com/products/dc-power-loads/dp800/`, 2025. Accessed: 2025-05-17.

[37] Uni-Trend Technology, "UT58A Specifications." `https://meters.uni-trend.com/product/ut58-series/#Specifications`, 2025. Accessed: 2025-05-17.

[38] Miro, "Miro, The visual workspace for innovation." `https://miro.com/`, 2025. Accessed: 2025-05-17.

A EPS-v2 Size Constraints



B EPS architectures

The figure 23 contains the logical drawing of the architecture of the EPS-v1 and of the EPS-v1.1 created during this thesis. The program used for drawing the diagrams is Miro [38].

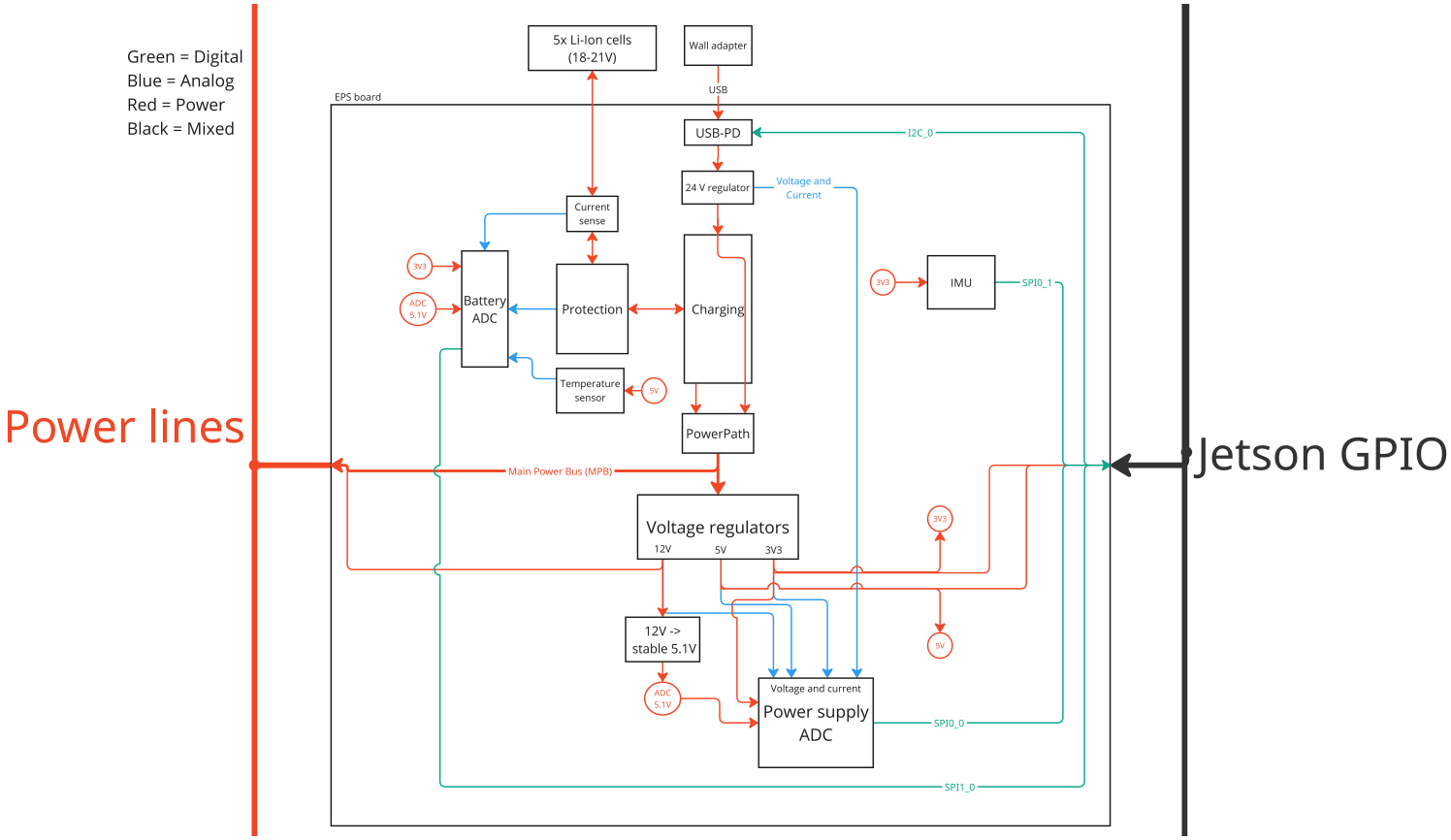
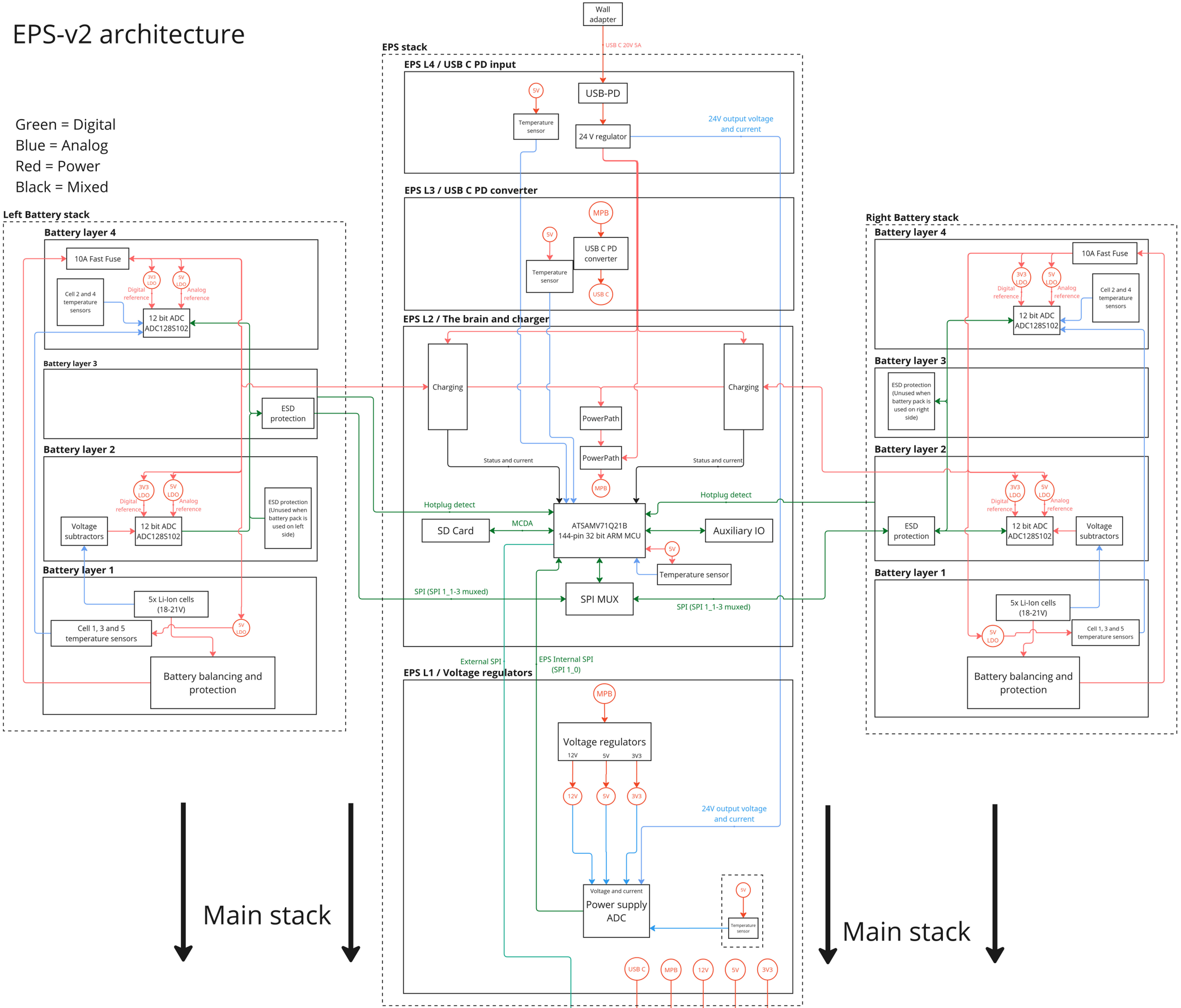


Figure 23: Logical drawing of the EPS-v1.1 architecture

On the following page EPS-v2 full architecture is drawn on a single figure.

EPS-v2 architecture

Green = Digital
Blue = Analog
Red = Power
Black = Mixed



C Connector pinouts

Pin	Signal	Signal	Pin
1	MOSI+	GND	2
3	MOSI-	GND	4
5	GND	MISO+	6
7	GND	MISO-	8
9	CLK+	GND	10
11	CLK-	GND	12
13	GND	$\overline{\text{CS+}}$	14
15	GND	$\overline{\text{CS-}}$	16
17	CC1	GND	18
19	CC2	GND	20
21	GND	GND	22
KEY			
23	GND	GND	24
25	GND	GND	26
27	GND	GND	28
29	GND	GND	30
31	3V3	GND	32
33	3V3	GND	34
35	3V3	GND	36
37	GND	5V	38
39	GND	5V	40
41	GND	5V	42
43	12V	GND	44
45	12V	GND	46
47	12V	GND	48
49	GND	USB C out	50
51	GND	USB C out	52
53	GND	USB C out	54
55	MPB	GND	56
57	MPB	GND	58
59	MPB	GND	60
61	MPB	GND	62
63	MPB	GND	64

Table 2: Pinout Table for the EPS to main stack connector

Pin	Signal	Signal	Pin
1	+24V	GND	2
3	+24V	GND	4
5	GND	MPB (Main Power bus)	6
7	GND	MPB (Main Power bus)	8
9	GND	MPB (Main Power bus)	10
11	GND	MPB (Main Power bus)	12
13	GND	MPB (Main Power bus)	14
15	USB C Vout	GND	16
17	USB C Vout	GND	18
19	Layer 3 Tsense	Layer 4 Tsense	20

Table 3: Pinout Table of the EPS internal power bus

Pin	Signal	Signal	Pin
1	+5V	GND	2
3	GND	+3V3	4
5	MOSI_INT (Internal connection)	CC1	6
7	MISO_INT (Internal connection)	CC2	8
9	CLK_INT (Internal connection)	Layer 4 24V Isense	10
11	$\overline{\text{CS\_INT}}$ (Internal connection)	Layer 3 24V Isense	12
13	MOSI_EXT (External connection)	MOSI_EXT (External connection)	14
15	MISO_EXT (External connection)	MISO_EXT (External connection)	16
17	CLK_EXT (External connection)	CLK_EXT (External connection)	18
19	CS_EXT (External connection)	$\overline{\text{CS\_EXT}}$ (External connection)	20

Table 4: Pinout Table of the EPS internal signal bus

Pin number	Functionality
1	MPB
2	MPB
3	MPB
4	MPB
5	MPB
6	MPB
7	Not connected (Kept empty for safety)
8	Battery hotplug detection
9	SPI MOSI
10	SPI MISO
11	SPI clock
12	$\overline{\text{SPI CS0}}$ (Battery monitoring)
13	$\overline{\text{SPI CS1}}$ (Battery temperatures)
14	Not connected (Kept empty for safety)
15	GND
16	GND
17	GND
18	GND
19	GND
20	GND

Table 5: Pinout table for the EPS-Battery connector

Pin	Signal	Signal	Pin
1	Battery +	GND	2
3	Battery +	GND	4
5	Battery +	GND	6
7	Battery +	GND	8
9	Battery +	GND	10
11	Battery +	GND	12
13	Cell 1 voltage	Cell 2 voltage	14
15	Cell 3 voltage	Cell 4 voltage	16
17	Cell 5 voltage	Unprotected GND	18
19	SPI MOSI	SPI MISO	20
21	$\overline{\text{SPI CS0}}$ (Battery monitoring)	SPI SCLK	22
23	$\overline{\text{SPI CS1}}$ (Battery temperatures)	GND	24

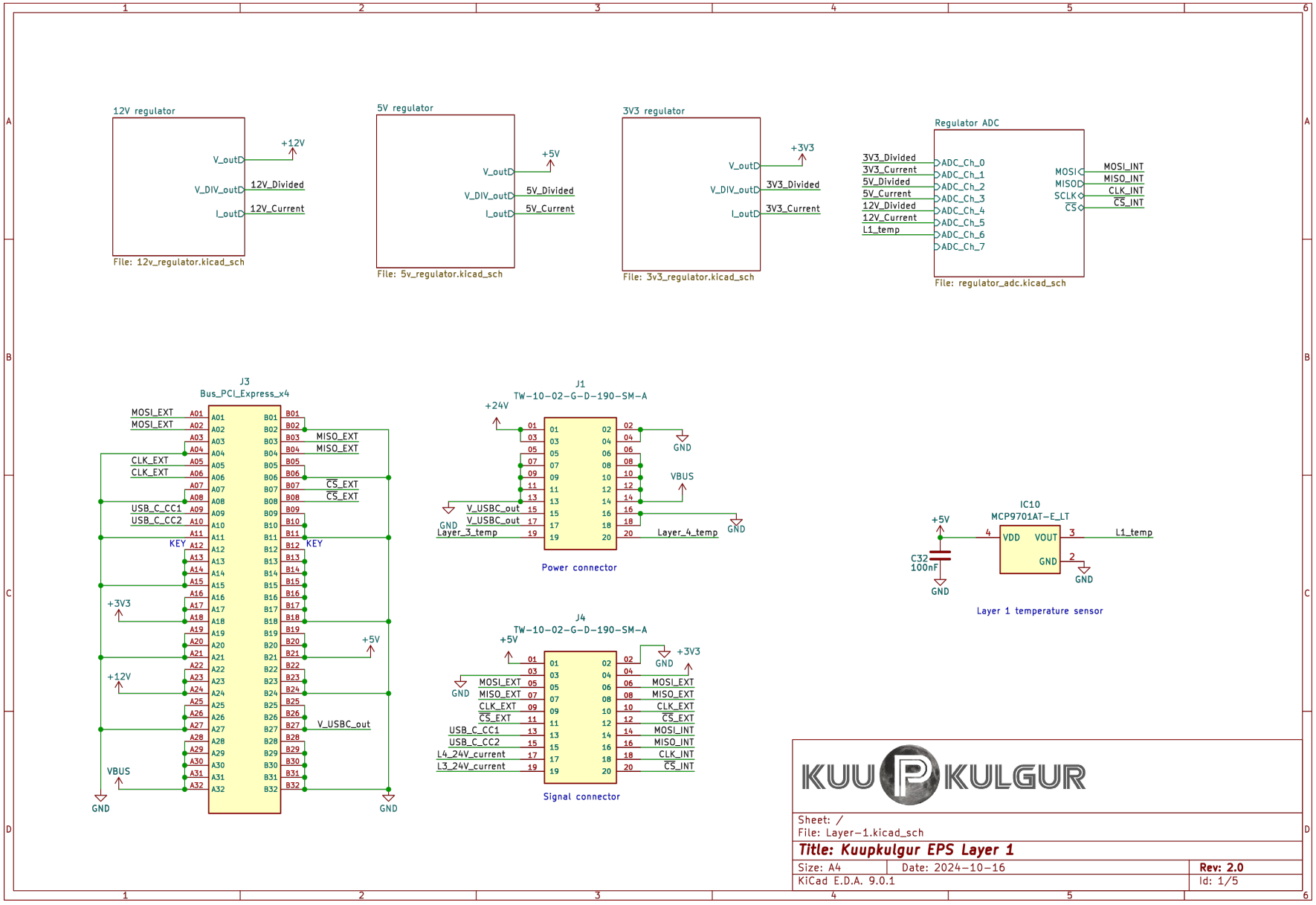
Table 6: Pinout Table of the Battery internal bus

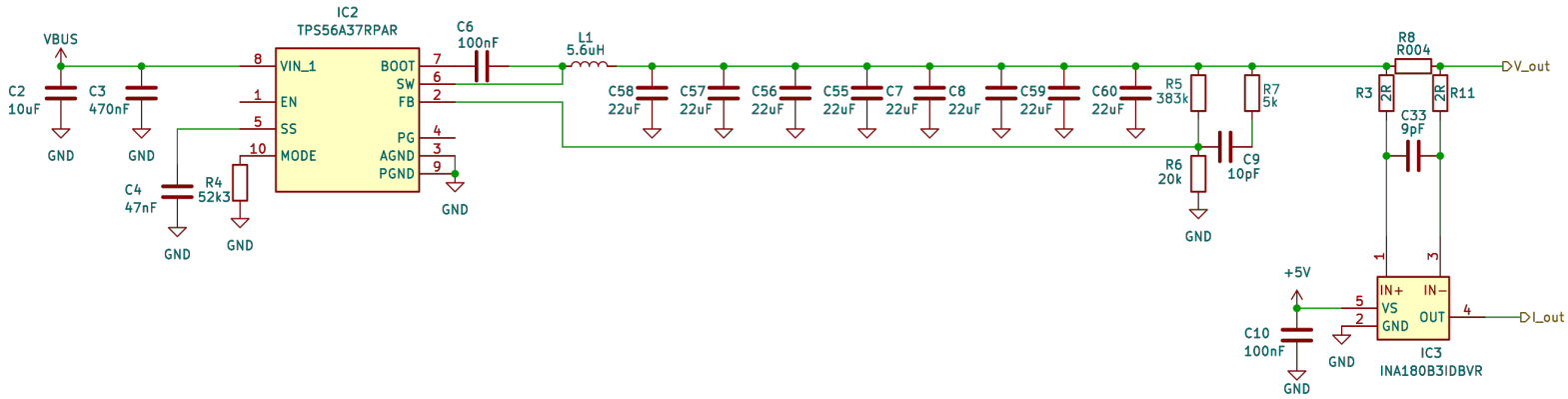
D EPS-v2 schematics

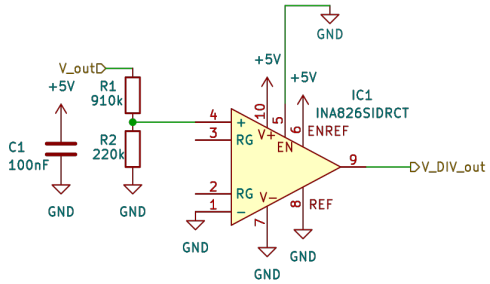
The following section presents the schematics created for the EPS-v2. The schematics are shown in the following order, beginning from the next page:

1. EPS Layer 1 – Voltage regulators
2. EPS Layer 2 – MCU and battery charger
3. EPS Layer 4 – USB-C Power Delivery input and to MPB converter
4. Battery pack Layer 1 – Battery balancing and protection circuitry
5. Battery pack Layer 2 – Voltage subtractors and measurement board
6. Battery pack Layer 3 – Symmetry layer for structural and routing balance
7. Battery pack Layer 4 – Temperature sensor ADC and fuse

D.1 EPS Layer 1 - Voltage regulators

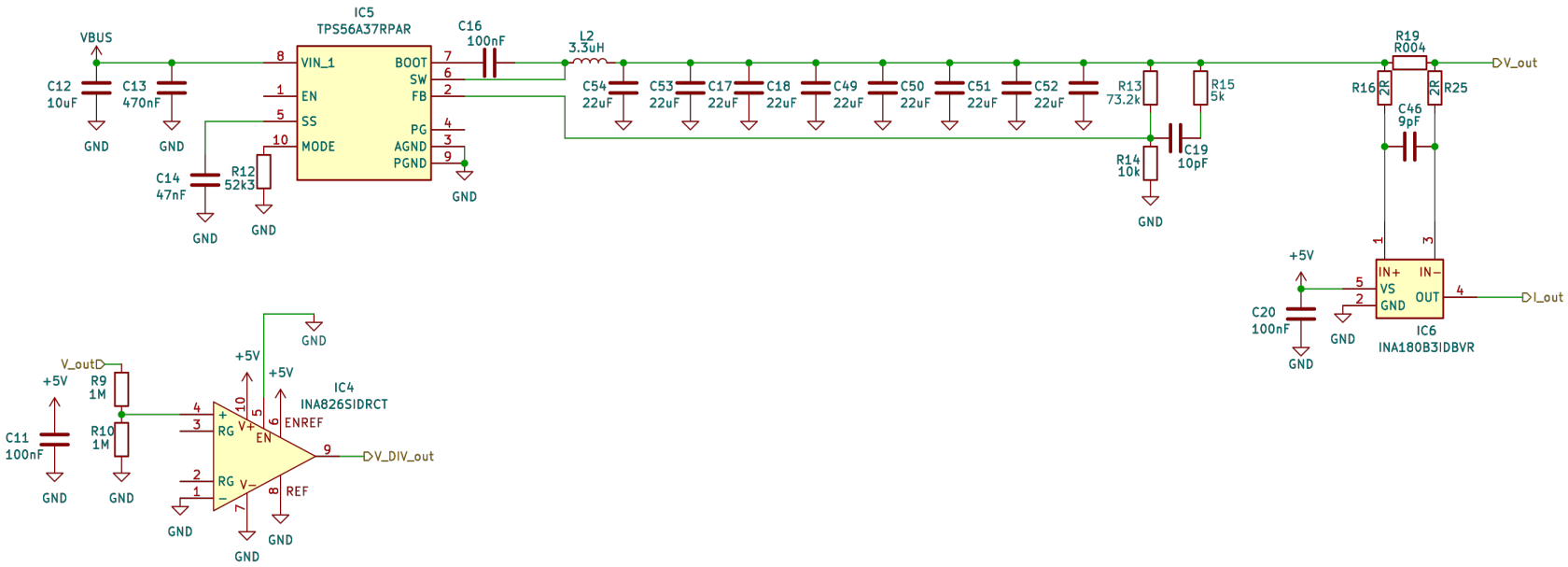






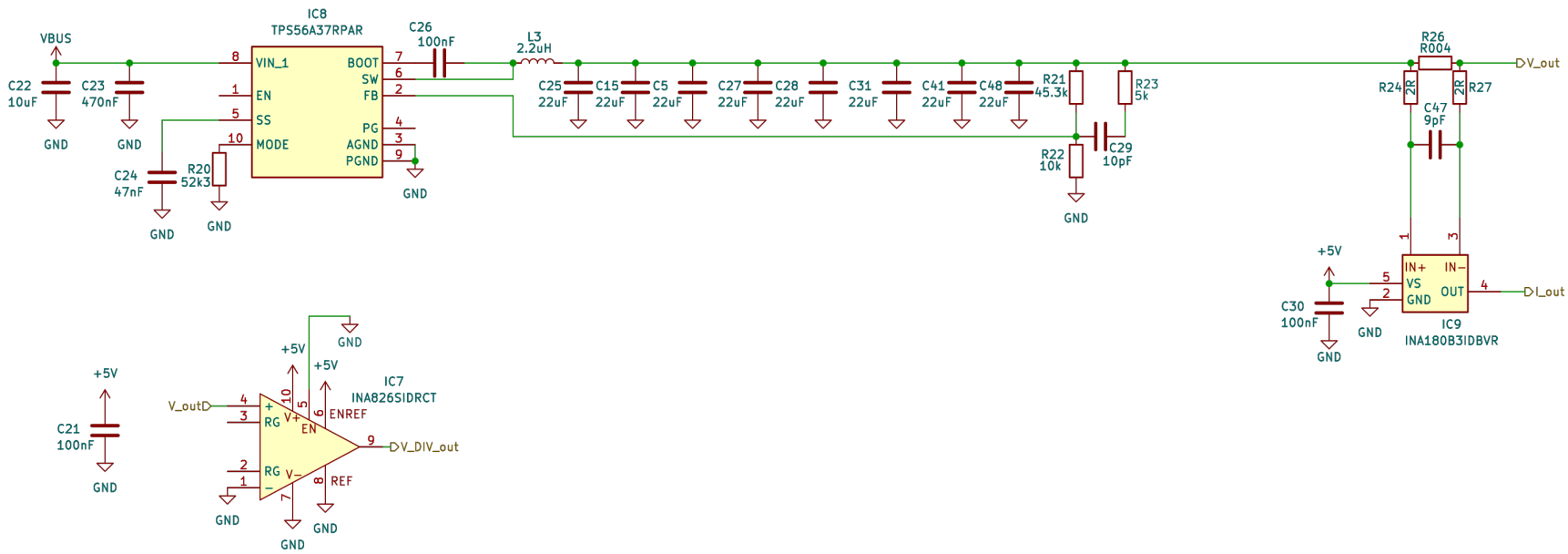
KUUPKULGUR

Sheet: /12V regulator/		
File: 12v_regulator.kicad_sch		
Title: Kuupkulgur EPS Layer 1		
Size: A4	Date: 2024-10-16	**Rev: 2.0**
KiCad E.D.A. 9.0.1		Id: 2/5



KUUPKULGUR

Sheet: /5V regulator/ File: 5v_regulator.kicad_sch		
Title: Kuupkulgur EPS Layer 1		
Size: A4	Date: 2024-10-16	**Rev: 2.0**
KiCad E.D.A. 9.0.1		Id: 3/5

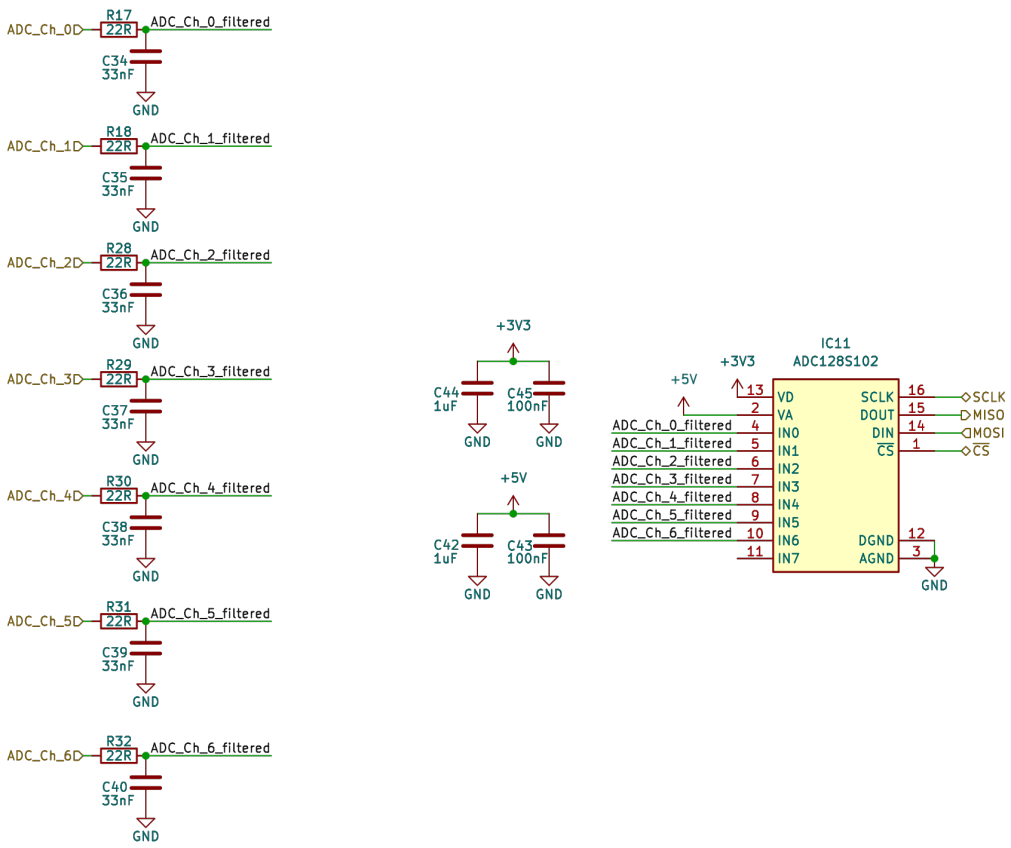


KUUPKULGUR

Sheet: /3V3 regulator/
File: 3v3_regulator.kicad_sch

Title: Kuupkulgur EPS Layer 1

Size: A4	Date: 2024-10-16	**Rev: 2.0**
KiCad E.D.A. 9.0.1		Id: 4/5



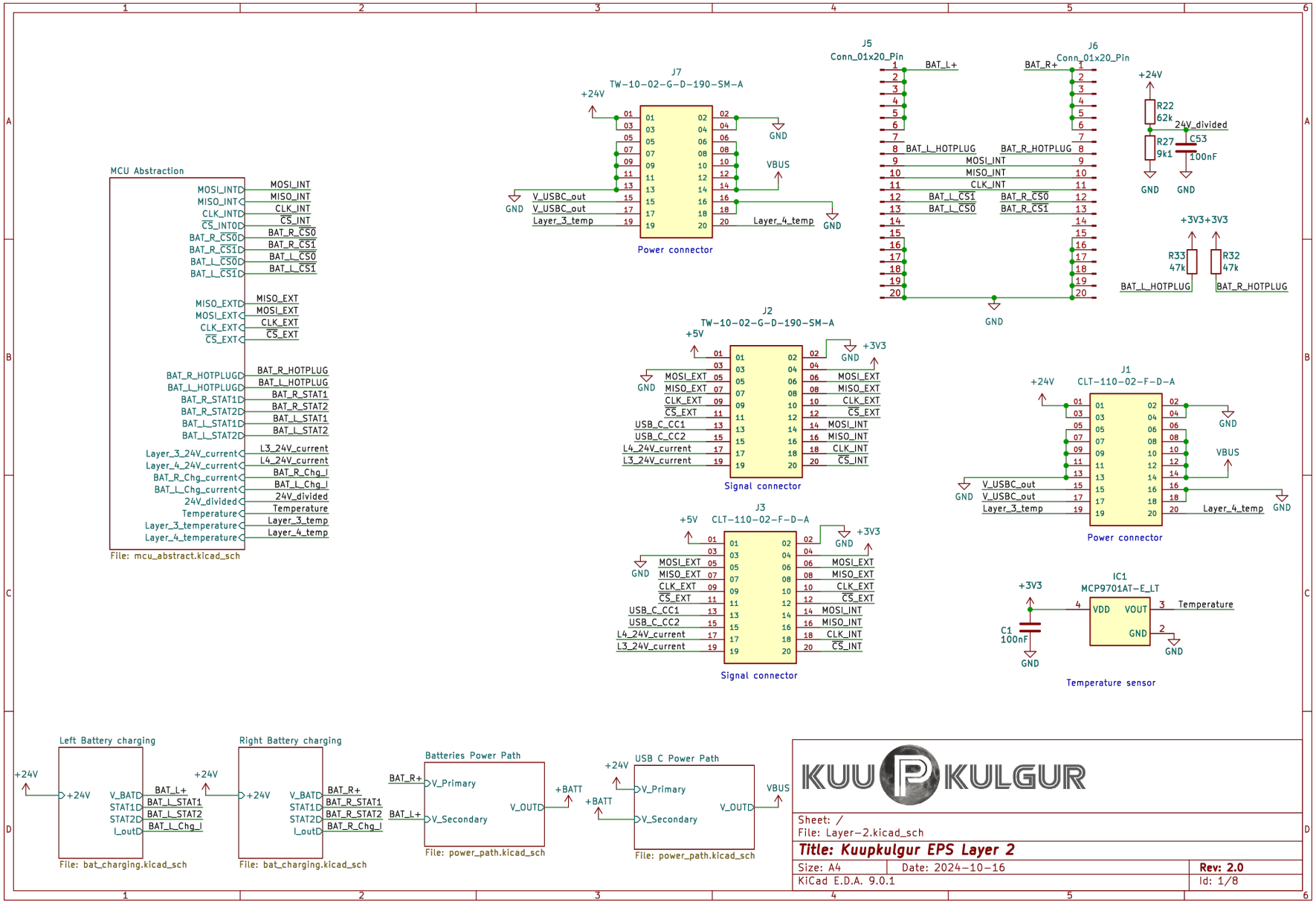
KUUPKULGUR

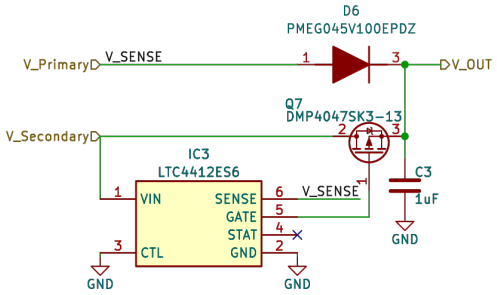
Sheet: /Regulator ADC/
File: regulator_adc.kicad_sch

Title: Kuupkulgur EPS Layer 1

Size: A4	Date: 2024-10-16	**Rev: 2.0**
KiCad E.D.A. 9.0.1		Id: 5/5

D.2 EPS Layer 2 -MCU and battery charger

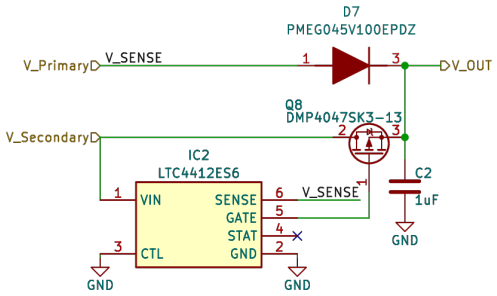




Power path switch

KUU PKULGUR

Sheet: /USB C Power Path/ File: power_path.kicad_sch		
Title: Kuupkulgur EPS Layer 2		
Size: A4	Date: 2024-10-16	**Rev: 2.0**
KiCad E.D.A. 9.0.1		Id: 2/8



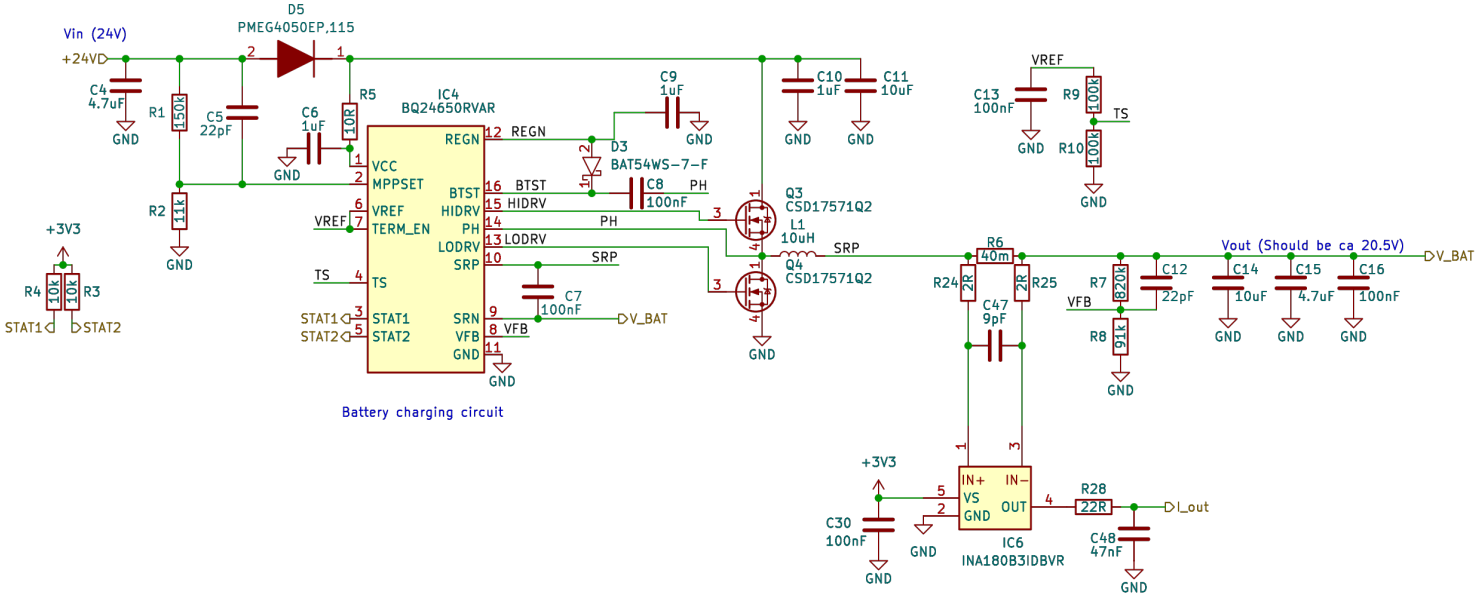
Power path switch

KUUPKULGUR

Sheet: /Batteries Power Path/
File: power_path.kicad_sch

Title: Kuupkulgur EPS Layer 2

Size: A4	Date: 2024-10-16	**Rev: 2.0**
KiCad E.D.A. 9.0.1		Id: 3/8

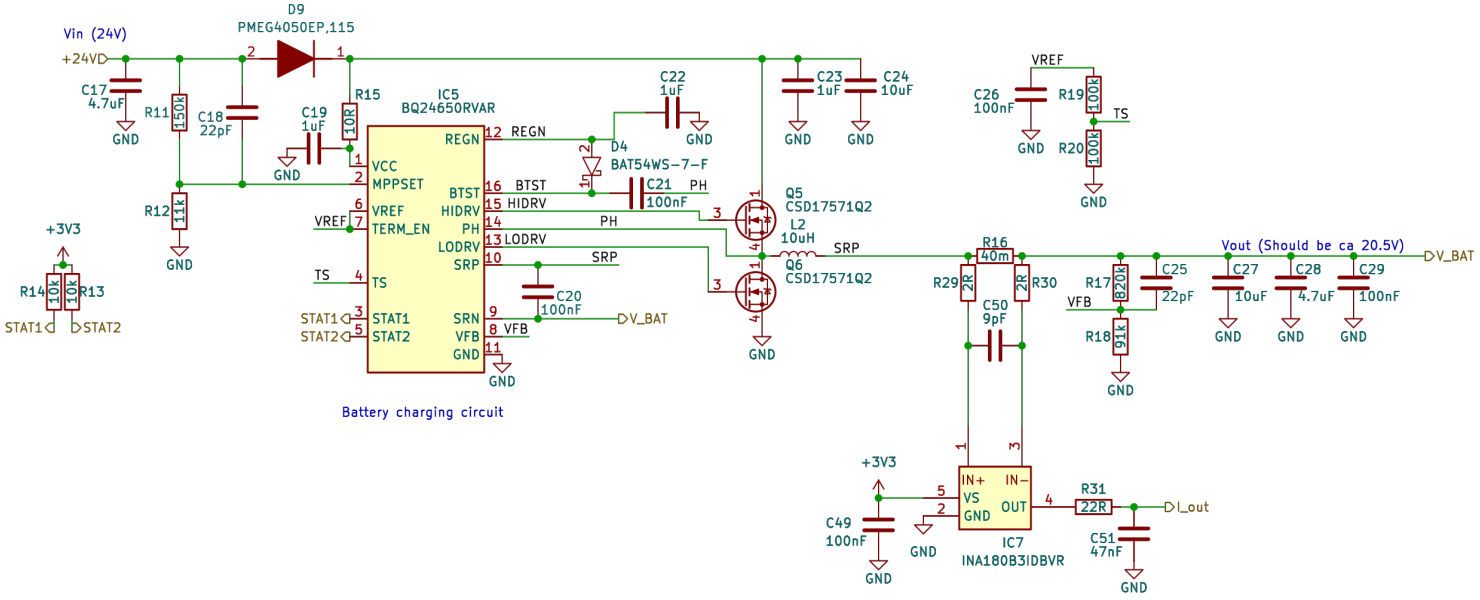


KUU KULGUR

Sheet: /Left Battery charging/
File: bat_charging.kicad_sch

Title: Kuupkulgur EPS Layer 2

Size: A4	Date: 2024-10-16	**Rev: 2.0**
KiCad E.D.A. 9.0.1		Id: 4/8

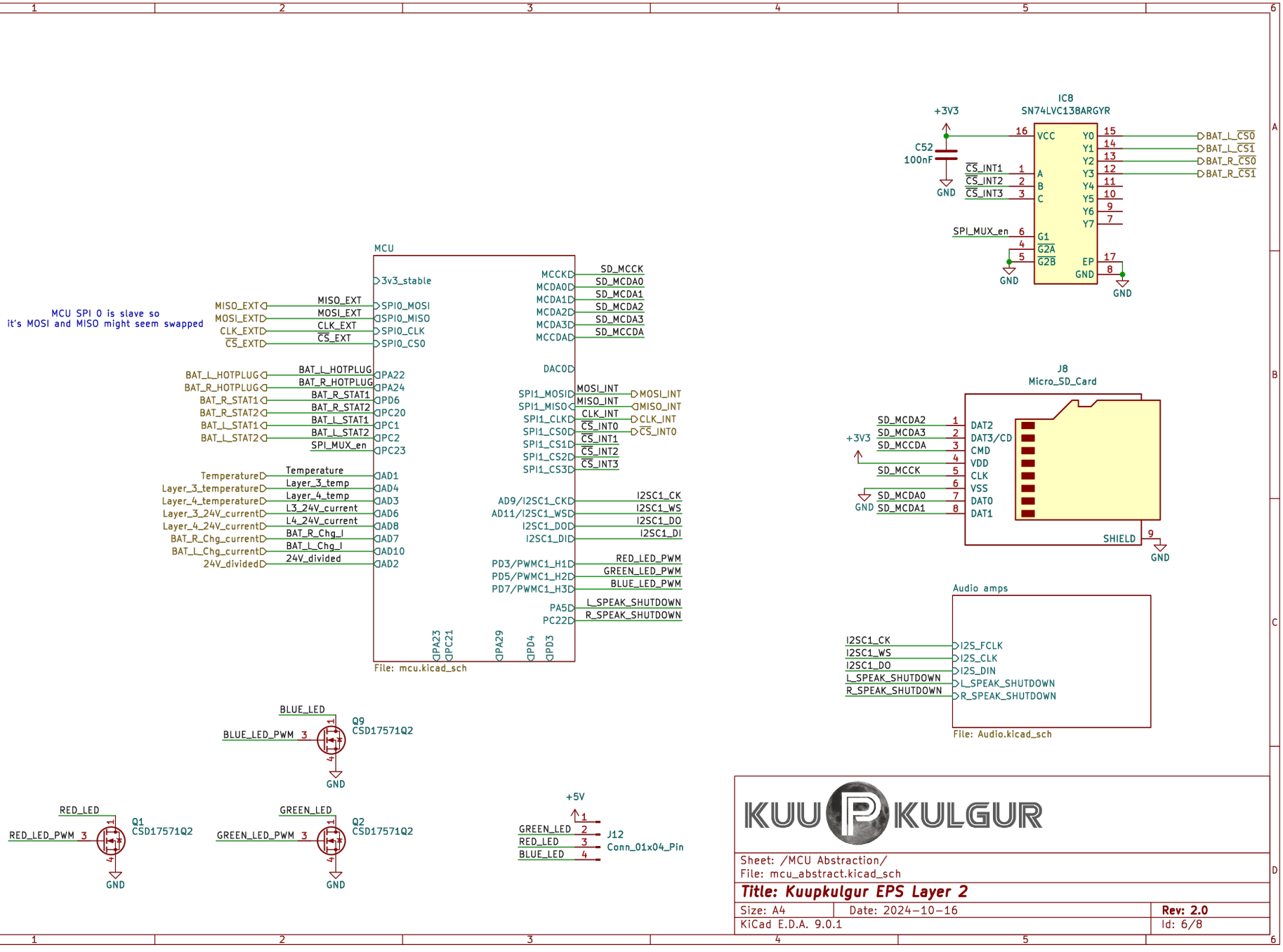


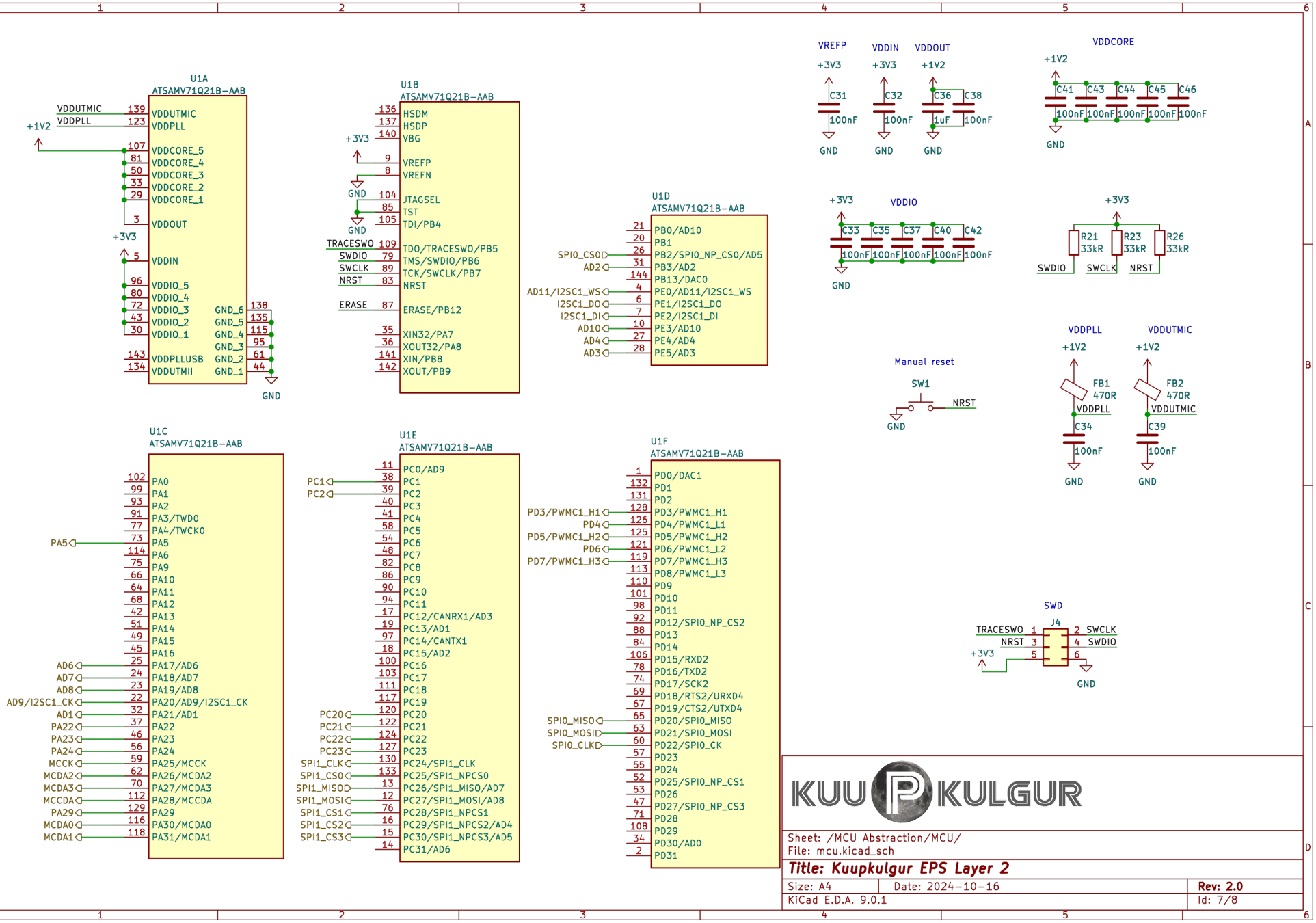
KUU KULGUR

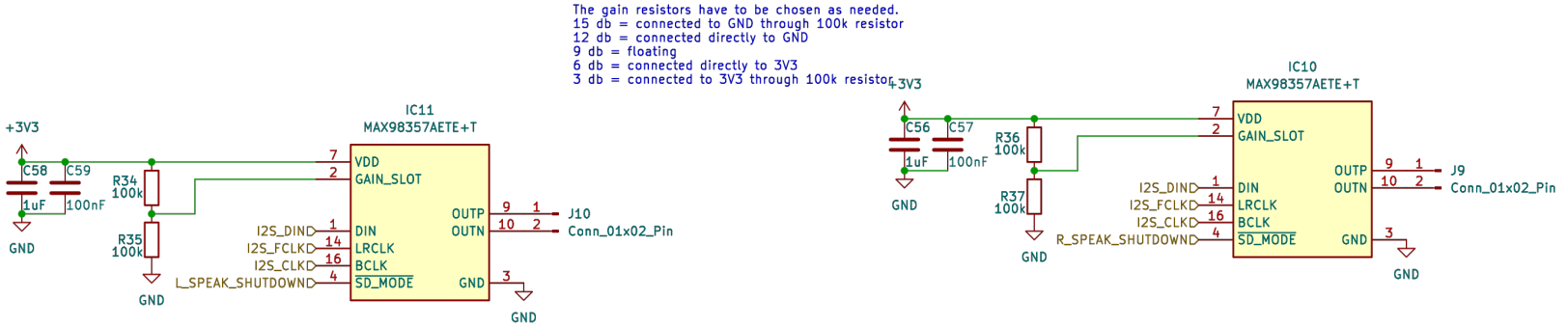
Sheet: /Right Battery charging/
File: bat_charging.kicad_sch

Title: Kuupkulgur EPS Layer 2

Size: A4	Date: 2024-10-16	**Rev: 2.0**
KiCad E.D.A. 9.0.1		Id: 5/8


MCU SPI 0 is slave so
it's MOSI and MISO might seem swapped
MCU
3v3_stable
MISO_EXT
MOSI_EXT
CLK_EXT
CS_EXT
SPI0_MOSI
SPI0_MISO
SPI0_CLK
SPI0_CS0
BAT_L_HOTPLUG
BAT_R_HOTPLUG
BAT_R_STAT1
BAT_R_STAT2
BAT_L_STAT1
BAT_L_STAT2
SPI_MUX_en
PA22
PA24
PD6
PC20
PC1
PC2
PC23
Temperature
Layer_3_temp
Layer_4_temp
L3_24V_current
L4_24V_current
BAT_R_Chg_I
BAT_L_Chg_I
24V_divided
AD1
AD4
AD3
AD6
AD8
AD7
AD10
AD2
MCCK
MCDA0
MCDA1
MCDA2
MCDA3
MCCDA
SD_MCCK
SD_MCDA0
SD_MCDA1
SD_MCDA2
SD_MCDA3
SD_MCCDA
DAC0
SPI1_MOSI
SPI1_MISO
SPI1_CLK
SPI1_CS0
SPI1_CS1
SPI1_CS2
SPI1_CS3
MOSI_INT
MISO_INT
CLK_INT
CS_INT0
CS_INT1
CS_INT2
CS_INT3
AD9/I2SC1_CK
AD11/I2SC1_WS
I2SC1_DO
I2SC1_DI
I2SC1_CK
I2SC1_WS
I2SC1_DO
I2SC1_DI
PD3/PWMC1_H1
PD5/PWMC1_H2
PD7/PWMC1_H3
RED_LED_PWM
GREEN_LED_PWM
BLUE_LED_PWM
PA5
PC22
L_SPEAK_SHUTDOWN
R_SPEAK_SHUTDOWN
PA23
PC21
PA29
PD4
PD3
File: mcu.kicad_sch
IC8
SN74LVC138ARGYR
+3V3
C52
100nF
GND
CS_INT1
CS_INT2
CS_INT3
A
B
C
G1
G2A
G2B
VCC
EP
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
BAT_L_CS0
BAT_L_CS1
BAT_R_CS0
BAT_R_CS1
J8
Micro_SD_Card
SD_MCDA2
SD_MCDA3
SD_MCCDA
SD_MCCK
SD_MCDA0
SD_MCDA1
DAT2
DAT3/CD
CMD
VDD
CLK
VSS
DAT0
DAT1
SHIELD
Audio amps
I2SC1_CK
I2SC1_WS
I2SC1_DO
L_SPEAK_SHUTDOWN
R_SPEAK_SHUTDOWN
I2S_FCLK
I2S_CLK
I2S_DIN
L_SPEAK_SHUTDOWN
R_SPEAK_SHUTDOWN
File: Audio.kicad_sch
BLUE_LED
BLUE_LED_PWM
Q9
CSD17571Q2
RED_LED
RED_LED_PWM
Q1
CSD17571Q2
GREEN_LED
GREEN_LED_PWM
Q2
CSD17571Q2
+5V
J12
Conn_01x04_Pin
KUU KULGUR
Sheet: /MCU Abstraction/
File: mcu_abstract.kicad_sch
Title: Kuupkulgur EPS Layer 2
Size: A4
Date: 2024-10-16
Rev: 2.0
KiCad E.D.A. 9.0.1
Id: 6/8


U1A
ATSAMV71Q21B-AAB
VDDUTMIC
VDDPLL
+1V2
VDDCORE_5
VDDCORE_4
VDDCORE_3
VDDCORE_2
VDDCORE_1
VDDOUT
+3V3
VDDIN
VDDIO_5
VDDIO_4
VDDIO_3
VDDIO_2
VDDIO_1
VDDPLLUSB
VDDUTMII
GND_6
GND_5
GND_4
GND_3
GND_2
GND_1
GND
U1B
ATSAMV71Q21B-AAB
HSDM
HSDP
VBG
+3V3
VREFP
VREFN
GND
JTAGSEL
TST
TDI/PB4
TRACESWO
SWDIO
SWCLK
NRST
TDO/TRACESWO/PB5
TMS/SWDIO/PB6
TCK/SWCLK/PB7
NRST
ERASE
ERASE/PB12
XIN32/PA7
XOUT32/PA8
XIN/PB8
XOUT/PB9
U1D
ATSAMV71Q21B-AAB
PB0/AD10
PB1
SPI0_CS0
AD2
PB2/SPI0_NP_CS0/AD5
PB3/AD2
PB13/DAC0
AD11/I2SC1_WS
PE0/AD11/I2SC1_WS
I2SC1_DO
PE1/I2SC1_DO
I2SC1_DI
PE2/I2SC1_DI
AD10
PE3/AD10
AD4
PE4/AD4
AD3
PE5/AD3
VREFP
VDDIN
VDDOUT
+3V3
+1V2
C31
C32
C36
C38
100nF
1uF
GND
VDDCORE
C41
C43
C44
C45
C46
VDDIO
C33
C35
C37
C40
C42
R21
R23
R26
33kR
Manual reset
SW1
NRST
VDDPLL
VDDUTMIC
FB1
FB2
470R
C34
C39
U1C
ATSAMV71Q21B-AAB
PA0
PA1
PA2
PA3/TWD0
PA4/TWCK0
PA5
PA6
PA9
PA10
PA11
PA12
PA13
PA14
PA15
PA16
AD6
PA17/AD6
AD7
PA18/AD7
AD8
PA19/AD8
AD9/I2SC1_CK
PA20/AD9/I2SC1_CK
AD1
PA21/AD1
PA22
PA23
PA24
MCCK
PA25/MCCK
MCDA2
PA26/MCDA2
MCDA3
PA27/MCDA3
MCCDA
PA28/MCCDA
PA29
MCDA0
PA30/MCDA0
MCDA1
PA31/MCDA1
U1E
ATSAMV71Q21B-AAB
PC0/AD9
PC1
PC2
PC3
PC4
PC5
PC6
PC7
PC8
PC9
PC10
PC11
PC12/CANRX1/AD3
PC13/AD1
PC14/CANTX1
PC15/AD2
PC16
PC17
PC18
PC19
PC20
PC21
PC22
PC23
SPI1_CLK
PC24/SPI1_CLK
SPI1_CS0
PC25/SPI1_NPCS0
SPI1_MISO
PC26/SPI1_MISO/AD7
SPI1_MOSI
PC27/SPI1_MOSI/AD8
SPI1_CS1
PC28/SPI1_NPCS1
SPI1_CS2
PC29/SPI1_NPCS2/AD4
SPI1_CS3
PC30/SPI1_NPCS3/AD5
PC31/AD6
U1F
ATSAMV71Q21B-AAB
PD0/DAC1
PD1
PD2
PD3/PWMC1_H1
PD4/PWMC1_L1
PD5/PWMC1_H2
PD6/PWMC1_L2
PD7/PWMC1_H3
PD8/PWMC1_L3
PD9
PD10
PD11
PD12/SPI0_NP_CS2
PD13
PD14
PD15/RXD2
PD16/TXD2
PD17/SCK2
PD18/RTS2/URXD4
PD19/CTS2/UTXD4
SPI0_MISO
PD20/SPI0_MISO
SPI0_MOSI
PD21/SPI0_MOSI
SPI0_CLK
PD22/SPI0_CK
PD23
PD24
PD25/SPI0_NP_CS1
PD26
PD27/SPI0_NP_CS3
PD28
PD29
PD30/AD0
PD31
SWD
J4
TRACESWO
NRST
SWCLK
SWDIO
KUU KULGUR
Sheet: /MCU Abstraction/MCU/
File: mcu.kicad_sch
Title: Kuupkulgur EPS Layer 2
Size: A4
Date: 2024-10-16
Rev: 2.0
KiCad E.D.A. 9.0.1
Id: 7/8



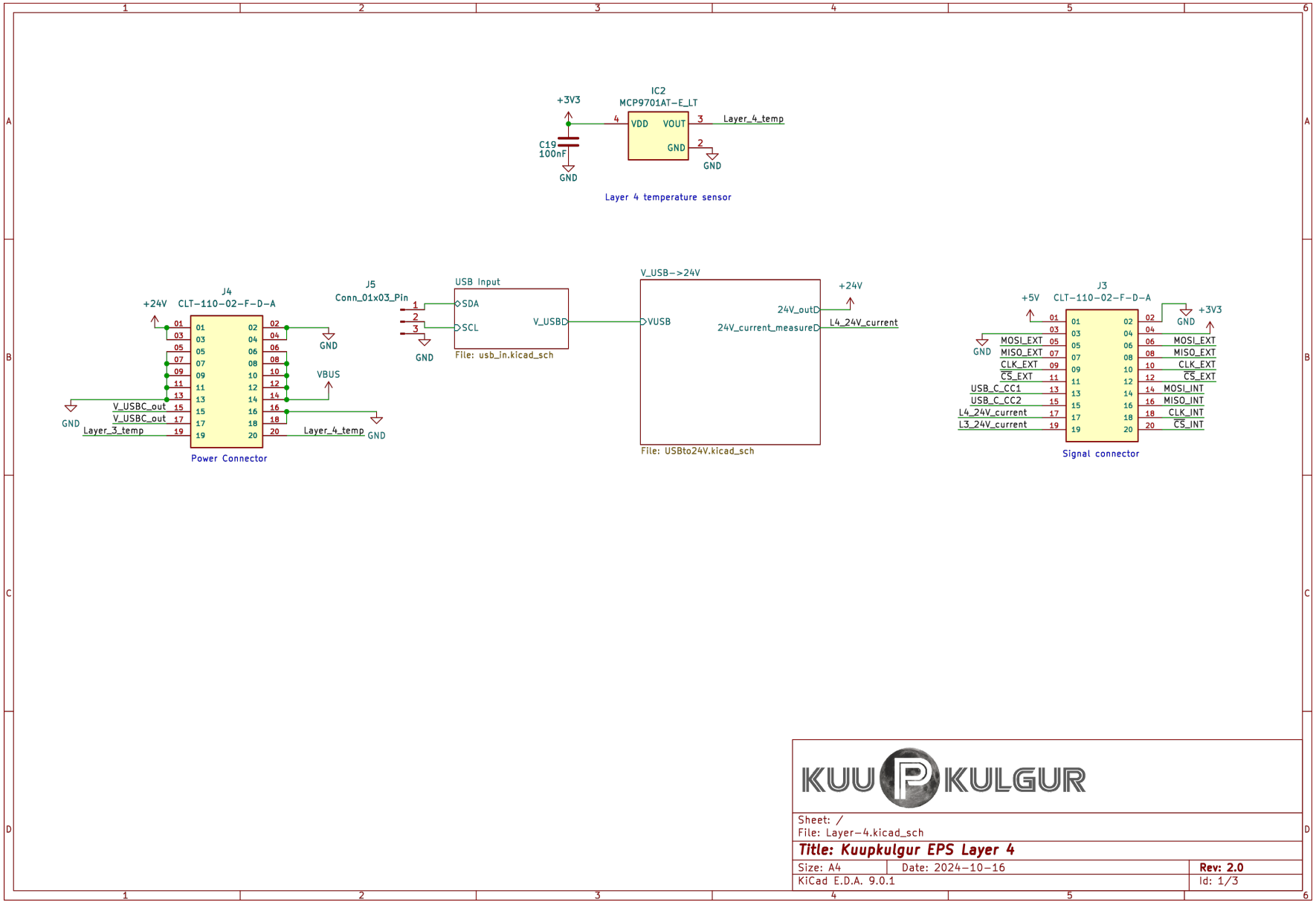
KUUPKULGUR

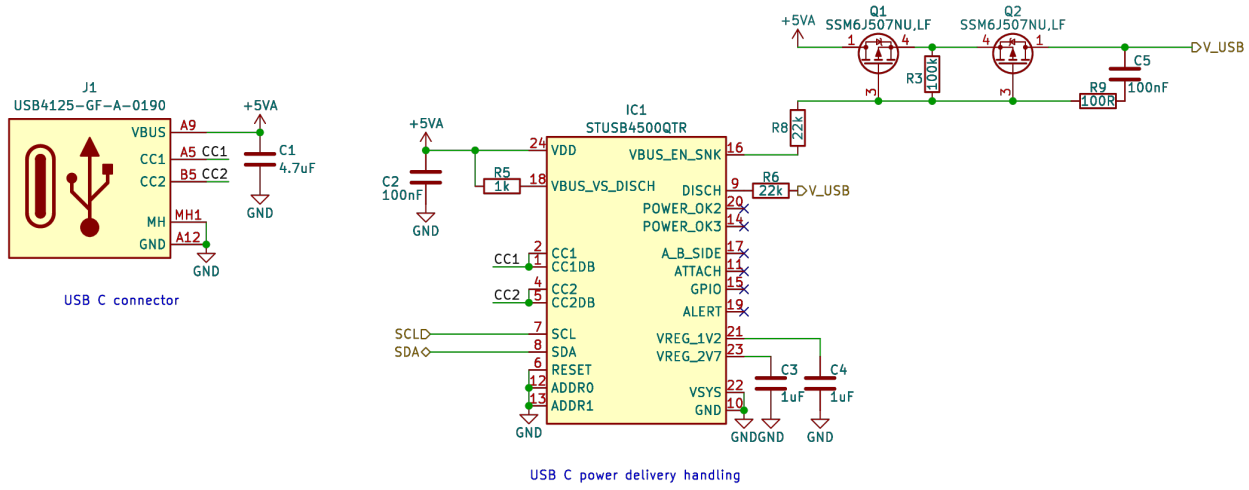
Sheet: /MCU Abstraction/Audio amps/
File: Audio.kicad_sch

Title: Kuupkulgur EPS Layer 2

Size: A4	Date: 2024-10-16	**Rev: 2.0**
KiCad E.D.A. 9.0.1		Id: 8/8

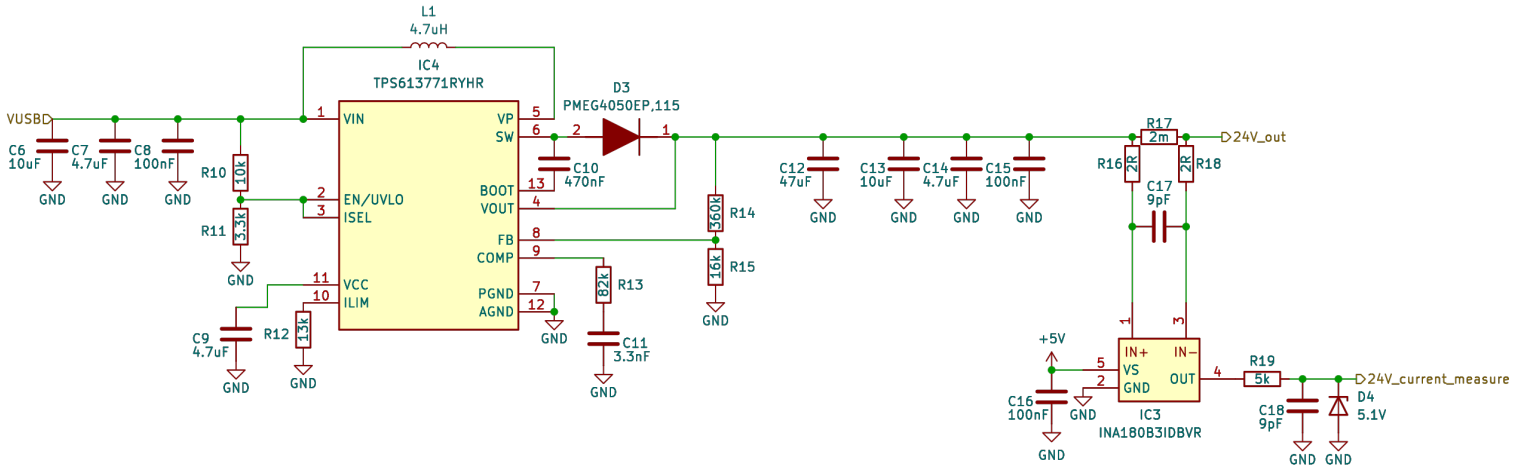
D.3 EPS Layer 4 - USB-C Power Delivery input and to MPB converter





KUUPKULGUR

Sheet: /USB Input/		
File: usb_in.kicad_sch		
Title: Kuupkulgur EPS Layer 4		
Size: A4	Date: 2024-10-16	**Rev: 2.0**
KiCad E.D.A. 9.0.1		Id: 2/3



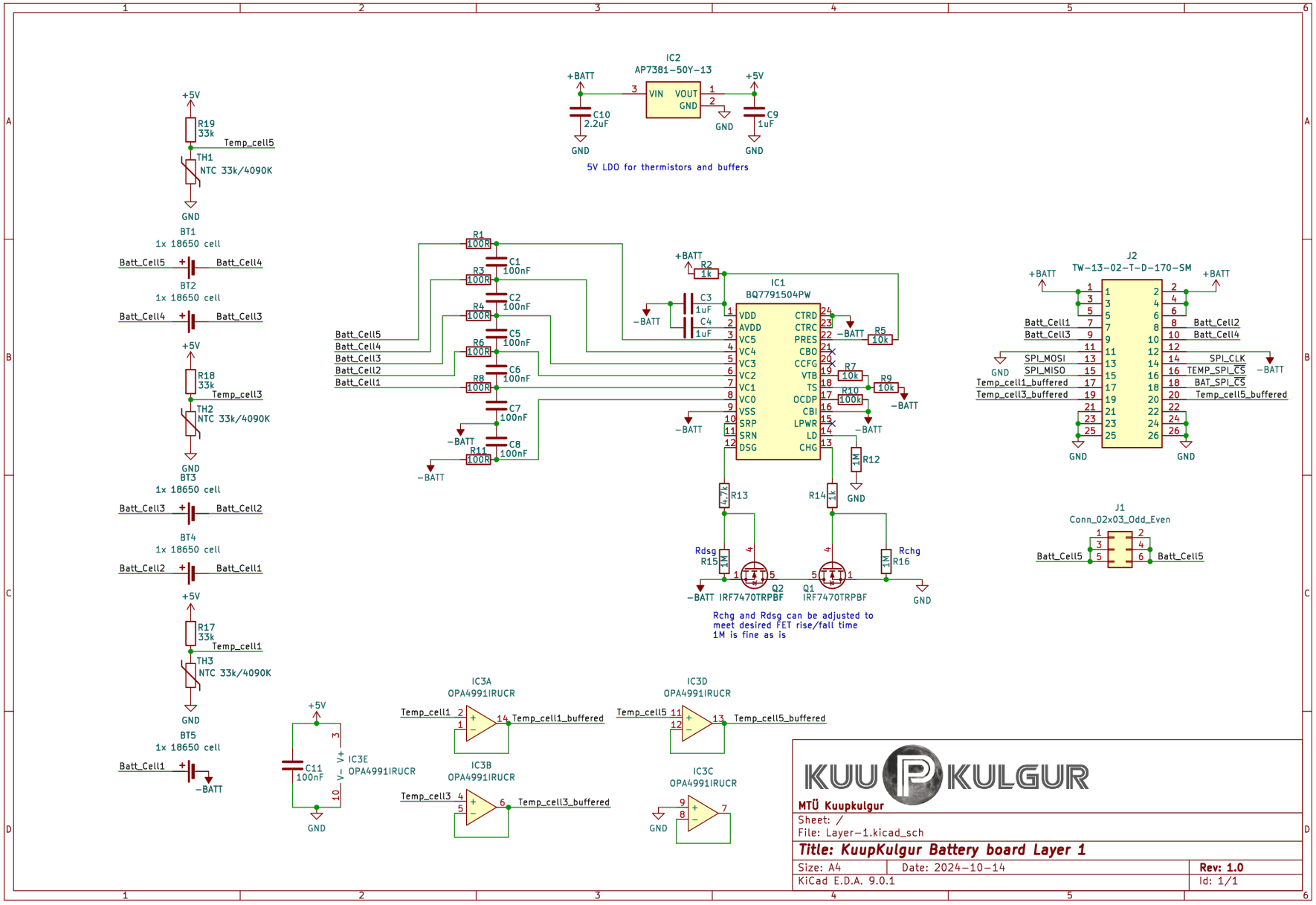
KUU KULGUR

Sheet: /V_USB->24V/
File: USBto24V.kicad_sch

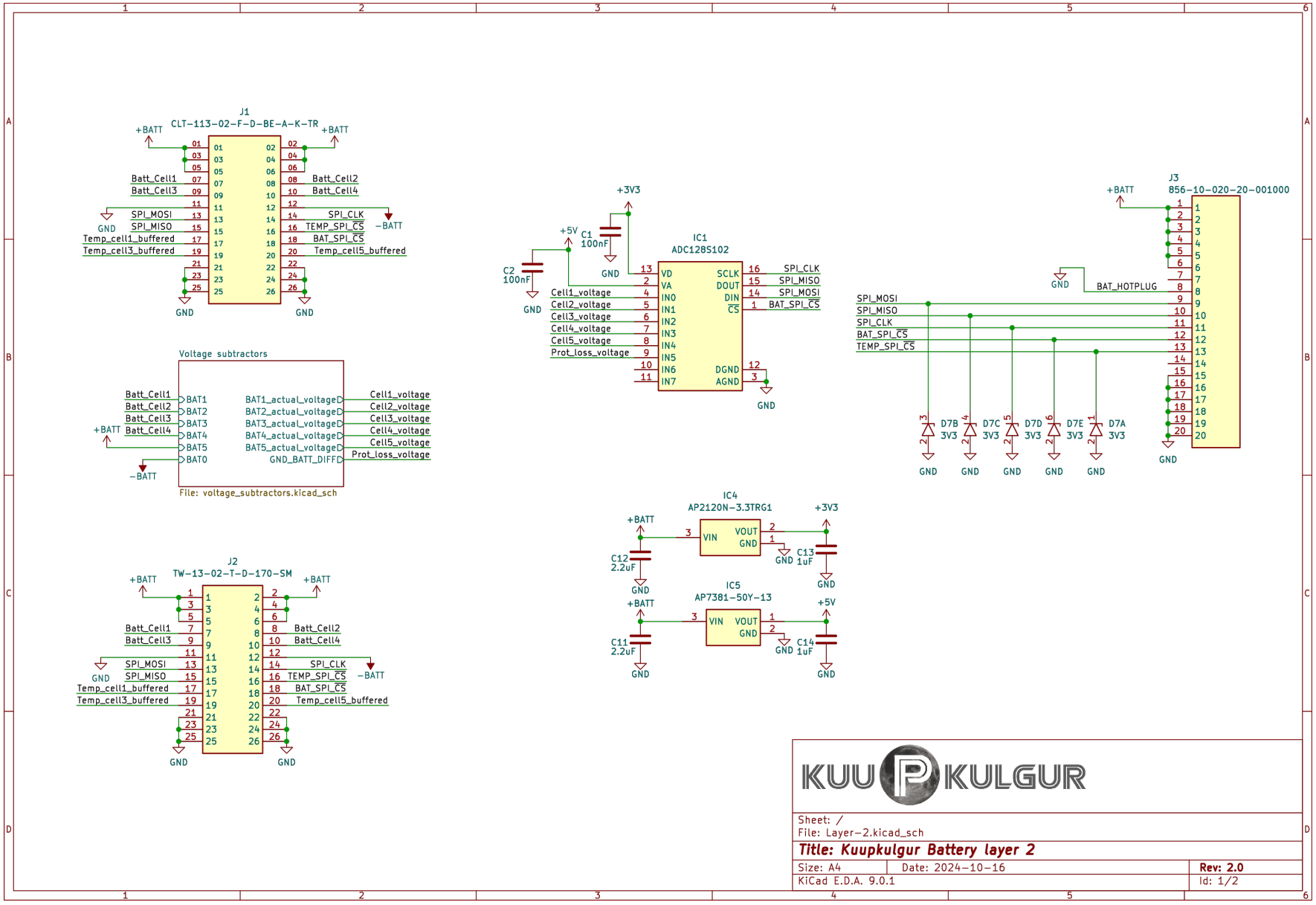
Title: Kuupkulgur EPS Layer 4

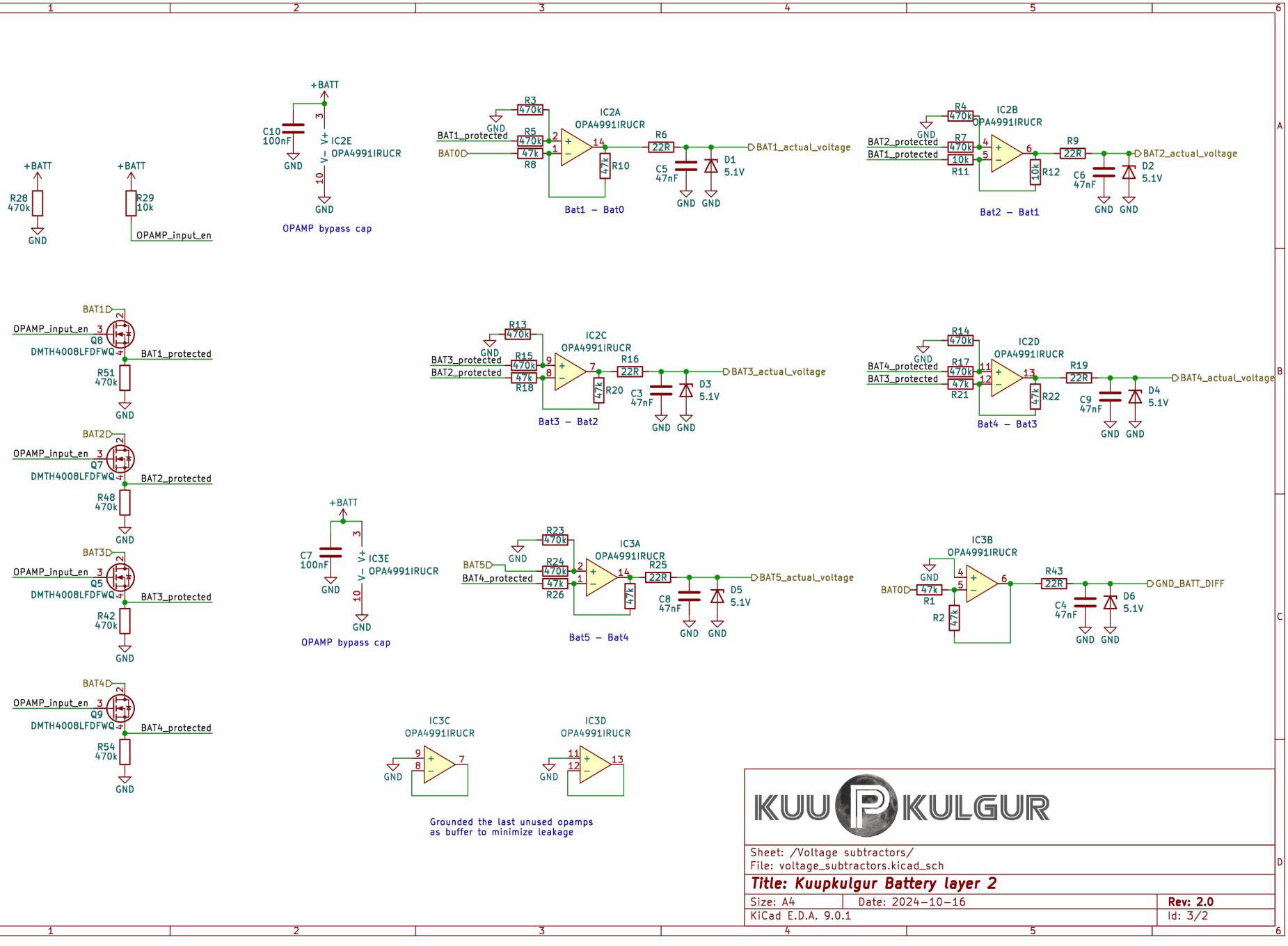
Size: A4	Date: 2024-10-16	**Rev: 2.0**
KiCad E.D.A. 9.0.1		Id: 3/3

D.4 Battery pack Layer 1 - Battery balancing and protection circuitry

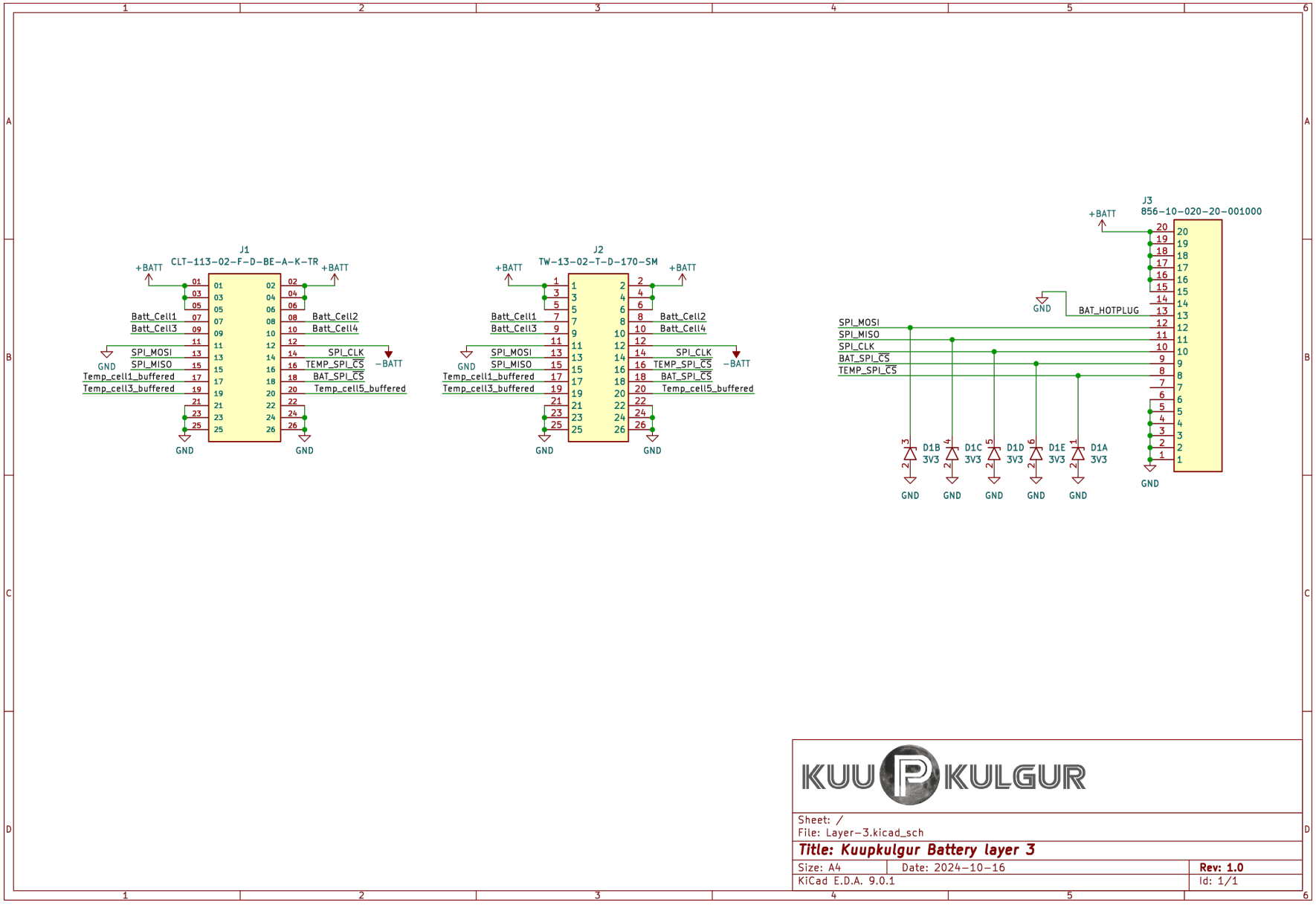


D.5 Battery pack Layer 2 - Voltage subtractors and measurement board

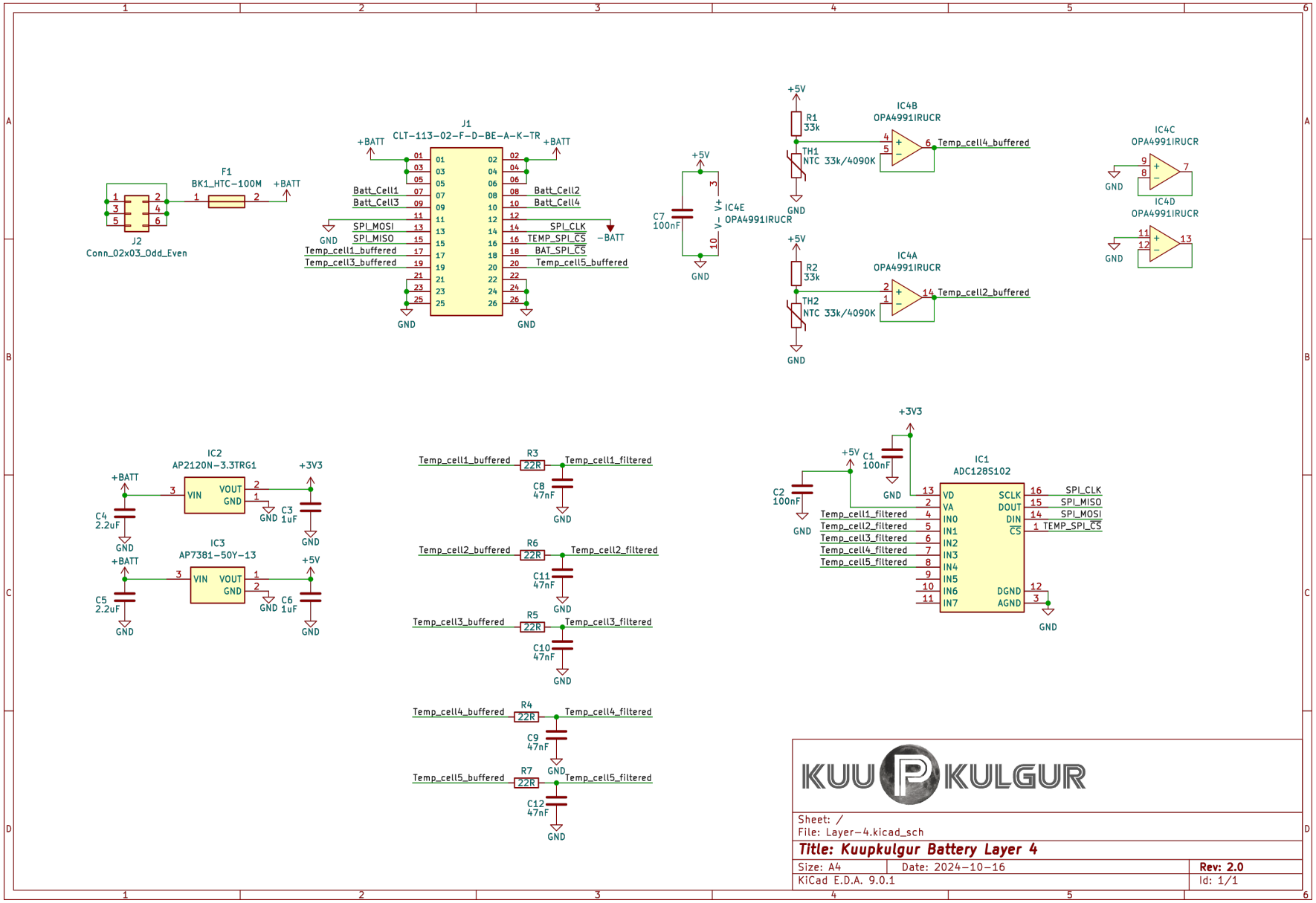



+BATT
R28
470k
GND
+BATT
R29
10k
OPAMP_input_en
+BATT
C10
100nF
GND
IC2E
OPA4991IRUCR
OPAMP bypass cap
R3
470k
GND
BAT1_protected
R5
470k
BAT0
47k
R8
IC2A
OPA4991IRUCR
R6
22R
BAT1_actual_voltage
47k
R10
C5
47nF
D1
5.1V
GND GND
Bat1 – Bat0
R4
470k
GND
BAT2_protected
R7
470k
BAT1_protected
10k
R11
IC2B
OPA4991IRUCR
R9
22R
BAT2_actual_voltage
10k
R12
C6
47nF
D2
5.1V
GND GND
Bat2 – Bat1
BAT1
OPAMP_input_en
Q8
DMTH4008LFDFWQ
BAT1_protected
R51
470k
GND
BAT2
OPAMP_input_en
Q7
DMTH4008LFDFWQ
BAT2_protected
R48
470k
GND
BAT3
OPAMP_input_en
Q5
DMTH4008LFDFWQ
BAT3_protected
R42
470k
GND
BAT4
OPAMP_input_en
Q9
DMTH4008LFDFWQ
BAT4_protected
R54
470k
GND
R13
470k
GND
BAT3_protected
R15
470k
BAT2_protected
47k
R18
IC2C
OPA4991IRUCR
R16
22R
BAT3_actual_voltage
47k
R20
C3
47nF
D3
5.1V
GND GND
Bat3 – Bat2
R14
470k
GND
BAT4_protected
R17
470k
BAT3_protected
47k
R21
IC2D
OPA4991IRUCR
R19
22R
BAT4_actual_voltage
47k
R22
C9
47nF
D4
5.1V
GND GND
Bat4 – Bat3
+BATT
C7
100nF
GND
IC3E
OPA4991IRUCR
OPAMP bypass cap
R23
470k
GND
BAT5
R24
470k
BAT4_protected
47k
R26
IC3A
OPA4991IRUCR
R25
22R
BAT5_actual_voltage
47k
C8
47nF
D5
5.1V
GND GND
Bat5 – Bat4
IC3B
OPA4991IRUCR
GND
BAT0
47k
R1
R2
47k
R43
22R
GND_BATT_DIFF
C4
47nF
D6
5.1V
GND GND
IC3C
OPA4991IRUCR
GND
IC3D
OPA4991IRUCR
GND
Grounded the last unused opamps
as buffer to minimize leakage
KUU KULGUR
Sheet: /Voltage subtractors/
File: voltage_subtractors.kicad_sch
Title: Kuupkulgur Battery layer 2
Size: A4
Date: 2024-10-16
Rev: 2.0
KiCad E.D.A. 9.0.1
Id: 3/2

D.6 Battery pack Layer 3 - Symmetry layer for structural and routing balance



D.7 Battery pack Layer 4 - Temperature sensor ADC and fuse



E Voltage regulator temperatures

The Figures 24 and 25 present the voltage regulator temperatures of the respective EPS at different output current levels.

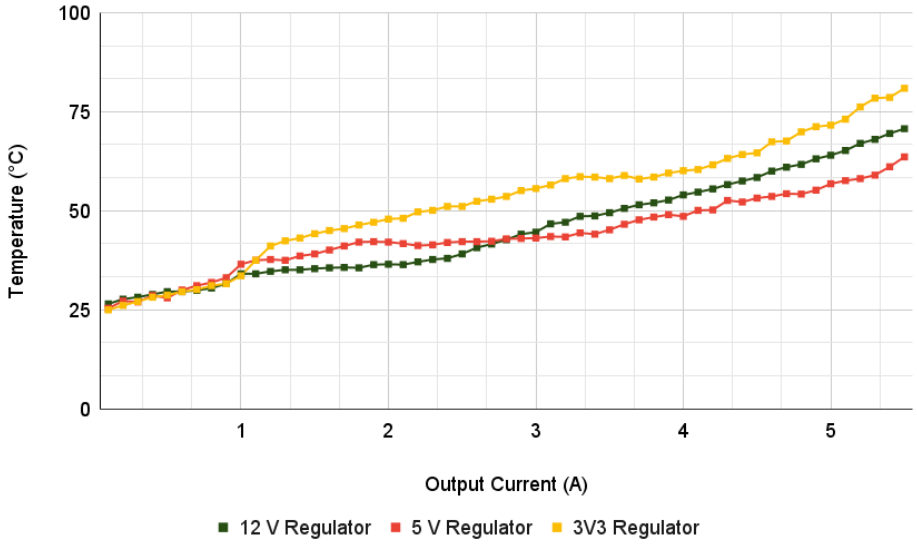


Figure 24: EPS-v1.1 temperatures during the stress test

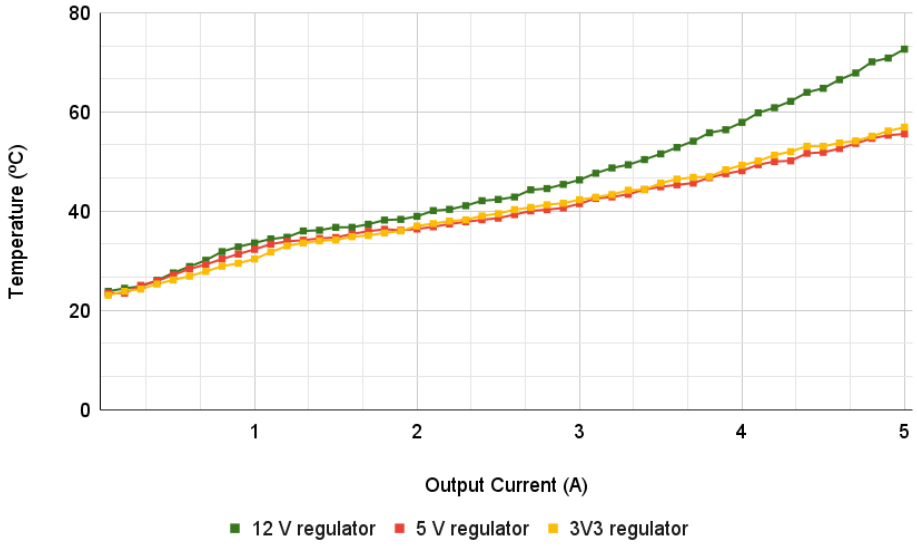


Figure 25: EPS-v2 temperatures during the stress test

Non-exclusive license to reproduce thesis and make thesis public

I, Laur Edvard Lindmaa

1. herewith grant the University of Tartu a free permit (non-exclusive license) to reproduce, for the purpose of preservation, including for adding to the DSpace digital archives until the expiry of the term of copyright,

   "Development of modular Electrical Power System for KuupKulgur prototype"

   supervised by Quazi Saimoon Islam and Mihkel Pajusalu

2. I grant the University of Tartu a permit to make the work specified in p. 1 available to the public via the web environment of the University of Tartu, including via the DSpace digital archives, under the Creative Commons license CC BY NC ND 3.0, which allows, by giving appropriate credit to the author, to reproduce, distribute the work and communicate it to the public, and prohibits the creation of derivative works and any commercial use of the work until the expiry of the term of copyright.

3. I am aware of the fact that the author retains the rights specified in p. 1 and 2.

4. I certify that granting the non-exclusive license does not infringe other persons' intellectual property rights or rights arising from the personal data protection legislation.

Laur Edvard Lindmaa
08/06/2025