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JOONAS MERISALU

Resistive switching in memristor structures with multilayer dielectrics

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Supervisors: Prof. Emeritus Jaan Aarik
Institute of Physics, University of Tartu, Tartu, Estonia

Prof. Kaupo Kukli
Institute of Physics, University of Tartu, Tartu, Estonia

Assoc. Prof. Aile Tamm
Institute of Physics, University of Tartu, Tartu, Estonia

Reviewer: Dr. Tatjana Dedova
Department of Materials and Environmental Technology,
Tallinn University of Technology, Tallinn, Estonia

Opponent: Dr. Robert Zierold
University of Hamburg, Center for Hybrid Nanostructures,
Hamburg, Germany

Commencement: Auditorium 121, Nooruse 1, Tartu, Estonia, at 13.15 on August 27th, 2024

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I. Conducting electrical measurements, analysis of results, formatting figures describing I-V characteristics, conducting XRF spectroscopy measurements supervised by P. Ritslaid, article draft writing.

II. Planning experiments, conducting ALD supervised by T. Jõgiaas, conducting electrical measurements assisted by T. D. Viskus and Mr. H. Chinedu, analysis of electrical characterization results and resistive switching properties, designing and formatting figures describing I-V characteristics, article draft writing.

III. Conducting electrical measurements, analysis of resistive switching properties and writing corresponding parts of the manuscript draft, formatting figures describing I-V characteristics, proofreading and amending the manuscript.

ABBREVIATIONS

AI	Artificial intelligence
ALD	Atomic layer deposition
BRS	Bipolar resistive switching
CBRAM	Conductive bridge random access memory
CCW-BRS	Counter clockwise bipolar resistive switching
CF	Conductive filament
CMOS	Complementary metal oxide semiconductor
CPU	Central processing unit
CRS	Complementary resistive switching
CW-BRS	Clockwise bipolar resistive switching
DRAM	Dynamic random access memory
EBE	Electron beam evaporation
ECM	Electro-chemical metallization
eNVM	Embedded nonvolatile memory
FET	Field effect transistor
GIXRD	Grazing incidence X-ray diffraction
High-k	High-permittivity
HRSEM	High resolution scanning electron microscopy
HRTEM	High resolution transmission electron microscopy
IC	Integrated circuits
IoT	Internet of things
LCR	Inductance, capacitance and resistance meter
MIM	Metal-insulator-metal
OML	Optical maskless lithography
PCB	Printed circuit board
PCM	Phase change memory
PMMA	Polymethyl acrylate
PVD	Physical vapor deposition
RRAM	Resistive random access memory
RS	Resistive switching
SCM	Storage class memory
SMU	Source and measure unit (electrical measurements)
SRAM	Static random access memory
STEM	Scanning transmission electron microscopy
TCM	Thermo-chemical mechanism
TMO	Transition metal oxide
URS	Unipolar resistive switching
VCM	Valence change mechanism
XPS	X-ray photo spectroscopy
PEALD	Plasma enhanced atomic layer deposition

INTRODUCTION

The amount of data that computer systems use is constantly increasing because the large data analysis provides higher accuracy in broad range of applications and thus, more digital data has been collected over the digital era than ever before. Analysis of large data sets collected in the real time or over a long period gives useful information to notice the trends and factors that can be used to optimize the wanted outcomes. For instance, the sensory equipment used for automation and digital control is able to capture increasing amounts of data in a large spectrum of fields, e.g., in production, finance, security, medicine, agriculture sectors, etc. Especially, the real-time applications, for instance self-driving cars, need vast amounts of data to be stored and processed quickly to make correct decisions.

The rapidly growing amount of data has forced engineers and scientists to constantly increase the capacity and downscale the sizes of computer memory devices to pack more data in roughly the same or even smaller packages (e.g., mobile gadgets). Meanwhile marked efforts are made to keep the reliability and increase the speed of memory devices as the processing speed of processors is greater and increasing faster than that of memory devices [1].

In modern computers, memory can be categorized into several types. Firstly, there are volatile and nonvolatile memories. The volatile memories can keep the data only when powered while the nonvolatile memories store the data also when the power is removed. In classical computers with the Von Neumann architecture, the memory is moved closer to the central processing unit (CPU) to ensure higher speed of data exchange, which is an important parameter of electronic memories. The fastest memory in common use is static random access memory (SRAM) with read and write time ~1 ns [2]. SRAM is a volatile memory, usually composed of 6 transistors, which are latched such that high or low (bit 1 or 0) state is stored while the memory element is powered. While SRAM is powered it theoretically has unlimited state retention. SRAM is used inside processors as a cache memory, to which the CPU has the fastest access and the most critical data for processor operating is kept in SRAM. The main drawbacks of SRAM are its high price and relatively large dimensions due to 6 transistors in it. However, its main benefit stems from the robust design, fast operation and very high endurance ($>10^{16}$ cycles) [2,3].

The next memory type is dynamic random-access memory (DRAM). DRAM is used as the main memory located close to the CPU while the data is communicated over the main memory bus. DRAM is also a volatile memory. It is called dynamic because it is based on keeping the charge on the non-ideal capacitor with metal-insulator-metal (MIM) structure. Non-ideal means that there is always a leakage current through the insulator (dielectric) layer, hence to keep the dynamically changing charge constant on the capacitor it has to be rewritten (recharged) over a period of time that is typically 64 ms [4]. DRAM has immense endurance ($>10^{16}$ cycles) and the write and read times (~10 ns) are an order of magnitude higher than those of SRAM [2]. The contemporary DRAM cell architecture is

based on one transistor and one capacitor (1T1C) which makes it more compact and smaller than SRAM. The most advanced modern DRAMs have reached 10 nm class technology with capacitance around 10 fF whereas further downscaling is facing serious difficulties [5]. This is mainly because the charge on the capacitor depends on the size of the capacitor and further downscaling of the electrode area would cause lowering of the capacitance, which cannot be reduced much below 10 fF due to the reliability of data storing. Further downscaling requires applying thinner dielectric layers that causes the increase in dielectric leakage currents, which requires an increase in the refresh frequency and, thus, increases the power consumption.

Lastly a mature electronic memory technology, relevant to this thesis is the flash memory (FLASH), which is nonvolatile and mostly used as a storage class memory (SCM). FLASH is based on the floating-gate field-effect transistor (FET). When writing voltage is applied to the gate electrode, hot electrons are injected from the transistor channel by electron tunneling effect (so called Fowler–Nordheim tunneling) are trapped in the floating gate. The floating gate is a virtual gate because it is isolated from the gate electrode and conduction channel of FET by dielectric layers. The electrons trapped on the isolated floating gate influence the voltage necessary to activate a FET conduction channel. Thus, the differences in voltages needed for the FET activation enable distinguishing the memory states. There are two architecturally different flash memory configurations, NAND and NOR type FLASH memories coined from the Boolean logic operations. In the NAND FLASH the floating gate transistors are connected so that they can be accessed in series, enabling faster data writing as blocks of floating gate transistors can be written almost simultaneously. However, this architecture limits the reading speed (10 μs) of each specific memory element. Thus, NAND FLASH is mainly used for the data storage where the writing speed is essential, e.g., in memory cards, solid state drives (SSDs), etc. In NOR type FLASH, the floating gate transistors are connected so that they can be accessed in parallel making the reading operation faster (50 ns), but on the other hand slowing down the writing process of the data. The writing speeds of floating gate transistors of NAND and NOR type FLASH do not differ that much, being 100 μs – 1 ms and 10 μs – 1 ms, respectively. However, the access time to individual floating gate transistors, directly affecting the reading time for different operations depends on the architecture as described above. Like DRAM, the FLASH memories are facing difficulties with downscaling as the charge, stored on the floating gate, and the reproducibility of data reading decrease with decreasing gate area. For both technologies, three-dimensional (3D) architectures of memory cells have enabled further scaling at the expense of more sophisticated, time-consuming, and expensive production [6,7].

Because of the above-mentioned issues with downscaling of those mature technologies, scientists and industry put much effort in the development of new emerging memory technologies. One of the most promising emerging memory technologies is based on the resistive switching (RS) phenomenon and is known as resistive switching random-access memory (RRAM). Structurally simple

metal-insulator-metal (MIM) design, based on 2 metal electrodes separated by a thin dielectric layer, non-volatility of resistive memory states, and complementary metal oxide semiconductor (CMOS) compatibility make RRAM memory type highly attractive within scientific community and many large well-known electronic enterprises [8]. Furthermore, RRAM has entered into industrial level as, for example, several big enterprises like Panasonic, Fujitsu, Sony, Intel, Samsung, SanDisk, and Toshiba have already adopted RRAM in small-scale development and production in a market segment of embedded non-volatile memory (eNVM) [9,10].

The principal difference of RRAM from DRAM is the performance of the MIM dielectric, when a writing and erasing signals are applied. In DRAM the MIM structure is used as a capacitor while in RRAM a similar MIM structure is used as a resistor with a variable resistance [11]. It has been shown that an architecture of RRAM that can be based on one transistor and one MIM used as a memory resistor (1T1R) [12,13] is similar to that of DRAM. Thus, architecture of RRAM is also similar to DRAM. For this reason, the industry has in general the technological readiness to produce RRAM devices with the packing densities similar to those of DRAM devices. The most important difference of RRAM from other memory technologies is the working principle that is based on the possibility to reliably and reproducibly change the resistance of the insulator (dielectric) material in a MIM structure. The FLASH and DRAM charge storing reliability is strongly dependent on the physical sizes of the memory elements, limiting the further downscaling of those. In contrast, the working principle of RRAM is much more independent of the physical dimensions [14], allowing application of markedly smaller memory cells compared with those of DRAM and FLASH.

In its current technological readiness, RRAM is not suited as a substitute to DRAM yet, because RRAM still has endurance limitations compared to that of DRAM. RRAM has demonstrated endurance up to 10^{12} cycles, low operation voltages < 3 V and fast writing time < 10 ns [2,15,16]. For comparison, the endurance of DRAM has exceeded 10^{16} cycles as mentioned above. From another perspective, compared to 3D NAND FLASH memories which require writing voltages >10 V, with writing times > 10 μs and demonstrate endurance of < 10^6 cycles, RRAM is considered to be rather competitive memory technology [6]. Hence, RRAM chips are especially promising for high-density data storage technology [11,17]. Moreover, besides random-access memory technology, RRAM technology offers a lot of interesting applications in several other fields. Examples of plausible applications are neuromorphic hardware implementation for neural networking, implementations in Boolean logic gates, and embedded non-volatile memory (eNVM) applications replacing NOR type FLASH memories in microcontrollers, smartcards, etc., as the power consumption of RRAMs is relatively low. [16,18]. Low power-consumption is a general target in the electronic industry, especially for devices like memory cells as billions of cells are often used in one memory chip. For neuromorphic applications, a comparative figure is 10^{14}, which is the number expressing the approximate number of synapses in a biological brain [19]. Therefore, the further research and development of RS processes, for

instance, in search of novel material combinations with superior RS properties is of great practical importance as well as of scientific interest. Consequently, the academic and industrial societies have put a lot of effort into the development and studies on different RS materials and their composites attempting to improve the performance and reliability of RS devices.

The claim of the thesis is the possibility to form and measure reproducible resistive switching behavior in materials layers that are conventionally more suited for the application in DRAM devices. Novel material combinations, represented by nanolaminates, mixtures and solid solutions of TiO_2 and Al_2O_3, as well as ZrO_2 and Al_2O_3 were engineered, with their chemical, physical, and electronic properties thereafter evaluated. Complementarily, layered stacks of HfO_2 and graphene were devised, in order to examine whether it is possible to develop non-destructive deposition methods for continuous films as resistive switching media on potentially flexible, but chemically inert substrates. Essentially, the results of the present work demonstrated that the combinations of the given materials can act as resistive switching media whereby their characteristics can be modified and optimized by fine tuning the composition and structure of the nanolaminates and solid solutions.

The first chapter of the thesis describes the background of RS and a short overview of the methods used for the preparation and characterization of thin solid films for RS applications. The objectives of this thesis are specified in the second chapter. The third chapter describes the research methods, applied to obtain the results presented in this thesis, while the fourth chapter is devoted to the results and discussion. The main results of the study are summarized in the last chapter of the thesis.

1. BACKGROUND

1.1 Resistive switching

As mentioned in the Introduction Section, a RS device is a MIM structure composed of RS medium sandwiched between two electrodes. There is a broad range of semiconductor storage devices in which the material resistance can be changed. Resistance change can be caused by several effects, for instance, by the phase change from crystalline to amorphous and *vice versa*, magnetoresistive effect such as spin-transfer torque, leakage currents affected by electron trapping and detrapping, and ionic drift caused by electric stimuli, forming conductive filaments (CF) [20]. These conductive paths or filaments have been visualized by several research groups around the world [21–23]. The ionic drift causes local redox reactions and is often related to oxygen vacancies in transition metal oxides (TMO). In this work, RS was initiated and investigated in TMO-based structures. Thus, the RS mechanisms described in the thesis are focused on filamentary-type RS.

It is generally accepted that the CF formation in such RS materials is attributed to defects and moving the defects back and forth inside the material in nanoscale dimensions [16]. During the formation, a CF connecting the top and bottom electrodes is formed in the structure. By applying appropriate electric stimuli, the CF can further be disrupted and reconnected. Furthermore, the resistance of the material could also be programmed (switched) between several values (multi-level RS). It is worth noting in this connection that the stochastic nature of the defect movement significantly influences the RS processes and should be considered when interpreting the results of electrical measurements.

It has also been demonstrated that a single CF or multiple CFs can be formed in a RS memory cell [22,24]. Therefore, a question arises, how controllable is the size or number of these filaments. In general, the size of CF can be a mere fraction of the functional electrode area and, thus, it is rather difficult to study. The stochastics and multiple CFs are considered to cause unreliable RS, which leads to some concern of achieving an appreciably reliable performance of RS devices [25]. However, the nanoscale origin of CF is the main benefit for further downscaling the sizes of electronic memory cells and lowering the energy consumption of those. As an example, Pi *et al*. have demonstrated RS crossbar arrays with electrode areas of 2×2 nm^2, current below 10 nA per device, and data storing density in single layer design comparable to that obtained by stacking 64 layers of 3D NAND FLASH [14].

A RS device must have at least two controllable states. In RS devices, those two states are named low resistive state (LRS) and high resistive state (HRS). The transitions from HRS (state "0") to LRS (state "1") is usually denoted as the set procedure (SET) while the transitions from LRS to HRS is denoted as the reset procedure (RESET). The difference between the two resistive states, HRS and LRS, is termed as the memory window. In this work, the memory window is defined as a ratio of currents in LRS and HRS (I_{LRS}/I_{HRS}) at certain reading

voltage. The reading voltage is typically very low (ranging from –0.3 to 0.3 V) and does not affect the device state, i.e. reading operation is non-destructive.

From the device perspective, besides the memory window, the memory state retention duration, writing-erasing cycling endurance, as well as writing, erasing, and reading operation voltages (U_{SET}, U_{RESET} and U_{READ} respectively), time constraints, and power consumption are the most crucial parameters. The memory state retention demonstrates the non-volatility of HRS and LRS over a period of time. The resistance of these states may change, indicating the degradation of the CF [26]. Besides the number of total switching cycles, the endurance characteristic demonstrates how HRS and LRS resistance varies during sequential switching from HRS to LRS and from LRS to HRS. Due to the stochastic nature of the formation and disruption of CF, cycle to cycle variability of resistive states is one of the general problems of RS devices [27]. The stochasticity of RS is a main reason why RS devices are not yet in a large scale production for digital computer memories. All the previously mentioned parameters are especially crucial for the readiness of being used as a memory device and need special attention during the device optimization.

1.1.1 Electroforming

Electroforming or formation of CF is the first step of initiating RS. Depending on the type of RS, the electric field of a certain strength and polarity, applied to a pristine MIM memory cell, induces the first soft breakdown and the formation of CF. The first soft breakdown is described as formation because only a small portion of the filament is usually disrupted and reconnected during the further RS. Electroforming procedure can be conducted using a voltage or current source. When the behavior of a RS device is not known yet, it is more informative to conduct electroforming in the voltage source mode meanwhile limiting the maximum allowed current, i.e., the compliance current. In this way, one can identify the voltage and current value at which the forming event takes place. The current limitation is crucial to avoid hard (irreversible) breakdown. Later on, current sourcing can be used to initiate the forming process in other devices of the same sample because sometimes the current limitation in the voltage source mode is not reliable enough as benchtop source meters tend to overshoot the current due to parasitic capacitance before the feedback system detects a current value exceeding the limit [28,29]. This is connected to the peculiarity of dielectric breakdown, related to the abrupt current increase at the breakdown moment. For this reason, the current sourcing is preferred and often an external current limiting circuitry is added. In voltage sourcing mode, and while studying an unknown device, it is a good practice to start increasing current limit gradually until the first breakdown event [30]. This kind of rule of thumb helps to avoid accidental hard breakdown and initiate the device at minimum possible power consumption mode. In addition, for an applicable RS electronic device, the forming voltage and current must stay within acceptable error margins in the case of all memory cells to enable production of RRAMs industrially. Therefore, it is important to produce

RS media that have the cell to cell variance as low as possible. Several studies have demonstrated that some RS structures are forming-free, which is even more desirable for industrial application [31–33]. Forming-free means that the forming process takes place under the same conditions as the further switching of resistive states. However, achieving forming-free property of RS device can be viewed as further optimization of RS material structure that requires separate CF formation stage [34].

1.1.2 Resistive switching modes

1.1.2.1 Unipolar resistive switching

Unipolar resistive switching (URS) takes place at a certain electric field polarity, either positive or negative, with the SET operation taking place at a higher voltage value and RESET at a lower voltage value (Figure 1 a). The reasons for URS are complex. However, the most important attributor for URS is believed to be the Joule heating.

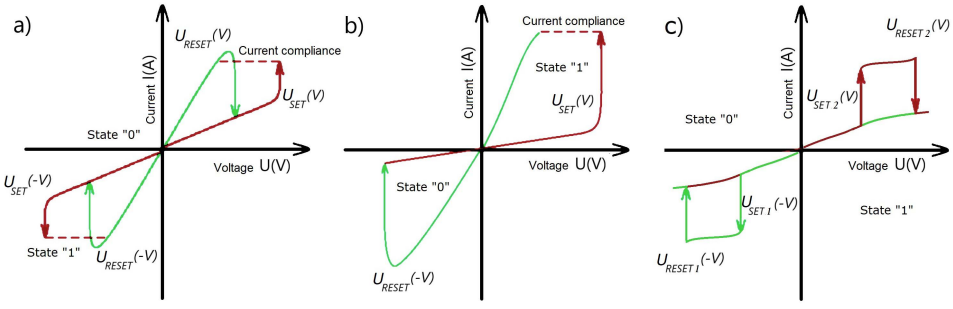

Figure 1. Schematic I-V characteristics of (a) unipolar resistive switching, (b) bipolar resistive switching and (c) complementary resistive switching devices.

To initiate the SET process, sufficiently high voltage has to be applied to achieve currents causing dielectric soft breakdown. In LRS, lower voltage of the same polarity, causing the RESET procedure, provides just enough energy for the so-called breakdown area to disrupt CF and switch the device to HRS. In this connection, it is important to notice that although the RESET procedure takes place at a lower voltage, the power required for successful RESET operation is usually higher than that required for SET procedure. Higher power is obtained at lower voltage because of much lower CF resistance and, correspondingly, much higher current flowing through the CF. The transition to HRS is a self-limiting process as the resistance increases reducing the current flow.

In the case of URS, the transition from LRS to HRS is mostly related to the thermochemical mechanism (that is discussed in Section 2.1.3.3). However the transition to LRS is sometimes related to metallic conduction and formation of metallic filaments in RS medium [35]. The latter peculiarity will be discussed in Section 1.1.3.1.

Unipolar RS with the single polarity operation seems to be more suitable for electronics as single-polarity power supplies are more common in electronic devices. At the same time, the temperature-dominated mechanisms are not that favorable in wide-band-gap dielectrics due to high probability for the hard breakdown. Nevertheless, URS memories have demonstrated promising endurance characteristics. For instance, Kang *et al*. [36] have described unipolar RS organo-metal halide perovskite media, capable of 10^8 endurance cycles.

1.1.2.2 Bipolar resistive switching

As the electric currents of the URS devices have been hard to be scaled down, the interest has shifted towards bipolar resistive switching (BRS) [16]. BRS is a type of RS where different polarities of electric field have to be applied for writing (SET) and erasing (RESET) operations. This means that certain voltage values (U_{SET}, U_{RESET}) with different polarities must be applied for these purposes. The devices working in the BRS mode are characterized by butterfly-looking I-V curves, when current is presented in the logarithmic scale. In more detail, BRS can be categorized as a clockwise BRS (CW-BRS) and a counterclockwise BRS (CCW-BRS, Figure 1 b). In the case of CW-BRS, the SET takes place at a negative bias and RESET at a positive bias while in CCW-BRS the SET operation takes place at a positive voltage and RESET occurs at the negative voltage polarity. A lot of prominent materials, e.g., HfO_2, can exhibit both CW-BRS and CCW-BRS, depending on the initial forming electric field polarity. For example, Vinuesa et.al. [37] have demonstrated that the preferential BRS direction may depend on the RS layer thickness. Therefore, it is important to understand how to optimize the BRS device to have one stable switching direction, as otherwise the endurance and overall performance can suffer from instability. From the endurance perspective, Kang *et al*. [36] have described organo-metal halide perovskite media with an endurance extending up to 10^{12} BRS cycles.

1.1.2.3 Complementary resistive switching

The third type of resistive switching, gaining also considerable attention, is called complementary resistive switching (CRS). This type of RS, addressing the sneak-path current problem in crossbar structures [38], can be observed in an anti-series connection of two BRS memristors. In this connection, one or another memristor is in HRS, so that the anti-serial couple is always highly resistive. This solution was initially proposed by Linn *et al*. [39] with two distinct BRS memristors sharing the same electrodes, one memristor working in clockwise and other in counterclockwise regime. Later it was discovered that there are materials expressing the same CRS in a single memristor with a specific layer design [40]. Here the anti-serial connection means that the two memristors are connected in opposite directions in terms of filament formation and disruption directions. In this connection, one memristor is operating in CW and another in CCW regime.

Although the design reduces the sneak-path current problem in crossbar structures, the read operation requires one of the memristors state being erased, which in turn, requires additional operation ($U_{RESET\,1}$ / $U_{RESET\,2}$, Figure 1 c) to restore the initial state [41,42].

1.1.3 Resistive switching mechanisms

This section will provide an overview of three generally agreed RS mechanisms, the valence-change mechanism (VCM), electrochemical metallization mechanism (ECM), and thermochemical mechanism (TCM) (Figure 2) that most significantly contribute to RS and therefore, can be used to explain why some materials attain RS [43]. The contributions of different RS mechanisms are not unambiguously understood yet, as different combinations of defects may promote various processes, related to electrochemical redox reactions and ion transport that may affect attaining RS [44–46]. Nevertheless, it is important to reckon the opinion that CF are formed in small areas of bulk material, where the energetic states are more strongly unbalanced compared to those in bulk material in general.

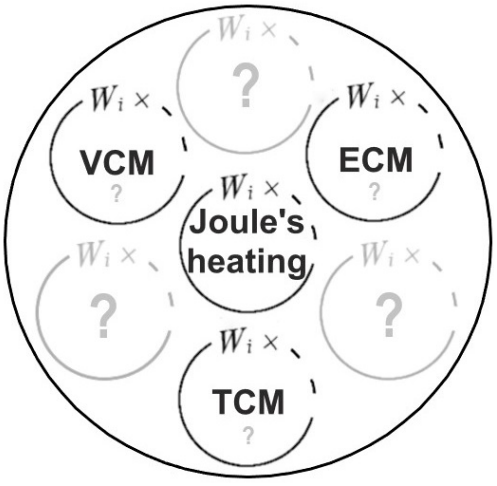

Figure 2. Probabilistic model of RS mechanisms, consisting of three commonly agreed mechanisms: valence change mechanism (VCM), electrochemical metallization mechanism (ECM), thermochemical mechanism (TCM). W_i denotes probabilistic weight function, determined for the *i*-th mechanism in experiments.

It should be noted that the co-existence of BRS and URS, observed in several studies [31,47–49], indicates that different mechanisms can simultaneously influence the RS processes while the probabilistic weight functions (W_i) of the mechanisms depend on the design of the RS cell and on the dielectric and electrode materials of the cell [50,51]. Furthermore, because of the small dimension of CFs Joule heating has an important role in all the three mechanisms that will be described in the following subsections.

1.1.3.1 Electrochemical metallization mechanism

The electrochemical metallization (ECM) mechanism could be described by analogy with electrochemical metal plating, where cations move from the anode (positive electrode) to the surface of a cathode (negative electrode) in a conductive liquid electrolyte, when a direct current bias is applied to the electrodes. In the RS device, the metal cations can similarly drift in the electric field from the chemically more active electrode (Cu, Ni, Ag, etc.) through the solid electrolyte i.e. RS layer (plausibly due to lattice defects and grain boundaries) and become reduced at a negatively charged passive electrode (Au, Pt, V, etc.) [52]. Nanoscale CF, containing significant amount of metal atoms, starts to form at the first sites, where the cations were reduced, and expands until it reaches the active electrode and, hence, connects the electrodes [44,52,53]. When the electric-field polarity is reversed, then the filament disrupts, plausibly at the active electrode, where the filament should have the smallest cross section and the current densities should reach the highest values. Further, following the same principle, the switching continues between the remainder of the filament and active electrode. It is hereby emphasized that electrodes play a key role in the ECM mechanism.

Instead of RRAM, a term conductive bridge RAM (CBRAM) has been used earlier to denote the devices based on ECM. CBRAM memory technology has been industrially pioneered by Adesto, now acquired by Dialog semiconductor offering the technology as eNVM for internet of things (IoT) and AI applications [54]. Although the RS devices, based on dominating ECM mechanism, initially suffered from poor cycling endurance related to high currents in transition from HRS to LRS, different additional ion barrier layers have proved to allow lowering the probability of device failure [55,56]. The most plausible reason for the device failure is the formation of conductive filaments, that are too large to be disrupted during the RESET process. Therefore, finding a RS medium design limiting the sizes of conductive filaments is important [57].

1.1.3.2 Valence change mechanism

Another well-known RS mechanism is the valence change one. Electrochemical reactions and ion migration, resembling ECM, are supposedly most significant to explain the valence change mechanism (VCM) [44]. The main difference of VCM from ECM originates from the moving species, i.e., VCM is based on the movement (migration) of oxygen ions and formation of oxygen related defects in oxides [53]. When an electric field is applied, the oxygen ions migrate towards positively charged electrode, leaving behind an oxygen-deficient path. Hence, it is more often referred to that the VCM is driven by the movement of oxygen-vacancies.

It is known that sub-oxides (Magneli phases) of some transition metals are conductive because in the electric field, the metal atoms of such sub-oxides partially coordinated to oxygen vacancies can release their valence electrons to the conduction band of the sub-oxide. Therefore, in these oxides, the movement of

oxygen ions (and oxygen vacancies), causing changes in the stoichiometry and valence states of cation sublattice, results in marked increase in conductivity [58]. Complementarily, different residual impurities (H, N, Cl, etc.), can exist in chemically deposited solid films. Hence, there might be even more migrating ions playing a role in the electrical conduction and formation of CF [59,60].

The disruption of CF would, again, be achieved by reversing the electric field polarity in the dielectric. As a result, the oxygen ions start to move back, filling the vacancies at least partially and, thus, disrupting the CF. The CF disruption usually takes place at one of the electrodes [58]. However, a problem arises when too many ions, which could contribute to the disruption, have formed strong bonds (mainly with electrode metal cations) at the dielectric-electrode interface. Hence, the disruption of CF may become impossible. To avoid this problem, chemically inert electrodes (Pt, Au, etc.) or appropriate interface layers embedded into the RS cell as oxygen reservoirs could be beneficial [61]. Alternatively, modified biasing scheme retaining the oxygen ions inside the RS medium [62] can be applied. In addition, choice of different electrode materials for the top and bottom electrodes can be beneficial to improve the performance of RS devices based on the VCM [63].

1.1.3.3 Thermo-chemical mechanism

In the case of TCM, the change in resistance is mainly caused by the temperature-induced defect diffusion related to intrinsic Joule heating. For instance, the temperature can accelerate the migration of oxygen vacancies and, therefore, influence the related redox processes. For this reason, to some extent, the Joule heating influences RS mechanisms described above. However, if the current can be conducted through a channel that is small enough and facilitates enough power, the temperature could raise sufficiently high [25] to cause even phase changes between crystalline and amorphous phase in the RS material. In the last scenario, the device is classified as the phase change memory (PCM).

In the RS devices based on TCM, the phase as well as stoichiometry of CF can change [64], while switching to both the LRS and HRS is possible by using the same electric field polarity. This means that URS is an indication of predominant TCM. Usually, electroforming of a TCM-based device with oxide-based RS medium is required to create oxygen-deficient CF with higher metallic cation (e.g., Ni in NiO) concentration, which results in metallic conduction of CF [64]. The filament concentrates the current and enables local heating causing temperature gradient inside the RS medium.

Strukov *et al.* [65] have proposed that Soret forces could cause the vacancies to group in the hotter region, enabling the SET process, when the temperature gradient is sufficiently high. The RESET process takes place, when there is more time for the dissipation of heat generated in the CF. In this case, the Fick diffusion, causing the oxygen ions around the filament to recombine with vacancies in CF, leads to the RESET process. In this sense, the switching kinetics of TCM is similar to that of PCM where the time parameters of switching pulses are generally used

to control the phase transitions [11]. One way or another, the temperature is the main parameter causing the formation and disruption of the CF alongside with the chemical redox transitions in the case of TCM [20]. Therefore, the memristors based on TCM, require rather high switching currents [64]. This is the main reason why these RS devices have attracted less interest than RS devices based on VCM and ECM mechanism.

1.1.4 Application of resistive switching in memory devices

While having at least two controllable and permanent resistive states in RS devices, one can attribute these states to bits "1" and "0", making RS phenomenon useful as a working principle of an electronic memory. Redox-reaction-based RS memory (ReRAM) [19], oxide-based RS memory (OxRAM), programmable metallization memory cell (PMC), phase-change memory (PCM), and conductive-bridge random access memory (CBRAM) are nuance-specific terms that are all coined to describe different types of RRAM. Among these memory types, PCM is the one that is mainly based on a specific class of materials, that is, chalcogenides.

Multilevel switching is one of the beneficial properties of RRAM. The importance of multilevel resistive switching is a possibility to exploit higher order numerical systems than just the binary one and, thus, make the data packing denser. For example, storing the decimal number 5 in binary (1 0 1) would need three memory cells holding bit values 1, 0, and 1. When using multilevel RS memory cells with three states, the decimal value of 5 could be stored in two memory cells holding bit values of 1 and 2 of the ternary numeral system (Table 1).

Table 1. The presentation of decimal numbers 1–5 in binary and ternary numeral systems demonstrating the number of memory cells necessary for storing the data.

Decimal representation	Binary representation	Ternary representation
1	1	1
2	10	2
3	11	10
4	100	11
5	101	12

From that example, it can be easily understood how the multilevel memories could enhance the data-packing density. Additionally, the potential of RS memory devices is related to programmable analog circuitry and newer concepts of computing in memory (integrating a processor and memory). The need in the latter concept arises from the increased power consumption and prolonged latency caused by the massive data movement between the memory and processor in the conventional von Neumann architecture. In the simplest case, the RS devices can

be combined as logic gates. Compared to CMOS logic gates, the RRAM gates could achieve higher density, lower power consumption and even higher speed [66]. Coming back to the multilevel operation of RRAM, the work of Liu *et al.* [67] describing RS-based ternary logic gates, allowing further reduction of the device sizes and power consumption, should be mentioned.

Neuromorphic processors are perhaps the most exotic application of RS devices. In this application, the combination of neural networks and analog electronics is used wherein the RS memristors mimic the synaptic behavior of human brain, acting as synaptic weights of neural network layers [68,69]. The latter application is important because of increasing demand for faster real-time computing that is, in turn, related to the need of instant image and sound recognition, necessary for the technology harnessing the artificial intelligence [69].

However, a significant technological issue with RS is related to the common way of producing memory structures with the crossbar electrode arrays consisting of word lines and bit lines. These RS crossbar structures are affected by so called sneak path currents, i.e., cross-talk interference due to elements that are in LRS on the selected word and bit line, that is a marked concern in the device-level integration [8,11]. There are several solutions like memory element design possibilities with active circuit elements like diodes or transistors. One can mention RS resistor and one diode (1D1R) architecture or one RS resistor and one transistor (1T1R) architectures, but the problem still needs attention [8].

1.2 Deposition and processing of thin-film structures

1.2.1 Atomic layer deposition

Atomic layer deposition (ALD) is one of the finest chemical vapor deposition methods, allowing the thin film thickness control with the sub-nanometer resolution and yielding appreciably homogenous structure and desired compositions of solid thin films [70]. Today it is one of the key technologies producing chips containing high-quality dielectrics as well as conductive material layers with CMOS compatibility [71]. Therefore, this method is a very attractive technique for deposition of RS media and electrodes of RRAM devices as well.

ALD is based on sequential self-limited surface reactions. The precursors are vaporized and, usually one at a time, carried by an inert gas (e.g., nitrogen) flow to a substrate where they alternately chemisorb and react with the solid surface. As a result, the solid medium grows in the layer-by-layer mode. This kind of approach avoids gas-phase reactions and, thus, results in the deposition of films with superior quality. Most frequently the thin solid films have been deposited at substrate temperatures exceeding 100 °C, although in some cases, the temperatures can be lowered down to room temperature, especially, when plasma-enhanced ALD (PEALD) has been used [72,73].

One of the key features of ALD is that the chemisorption of a precursor stops because of saturating and irreversible (i.e., self-limiting) reactions, when the

precursors, deposition temperature and precursor doses are properly chosen [74]. As a result, no more than one monolayer of species is usually added to the solid surface in one reaction step. In order to complete the synthesis of the film material and continue the deposition, the surface must be processed, e.g., by another precursor or several other precursors. This series of reaction steps, each of those followed by a purge period, forms an ALD cycle. As a rule, less than 0.2 nm film material is formed in a typical ALD cycle [70]. Thus, the ALD cycles must be repeated to obtain a thicker film in an ALD process. Provided that the conditions for the self-limiting adsorption of precursors are fulfilled, the thickness of a film depends on the number of ALD cycles performed rather than on the precursor doses and duration of the deposition process. For this reason, ALD also enables deposition of uniform and conformal thin solid films even on complicated 3D surfaces, which is especially important for semiconductor industry [72].

For the deposition of metal oxides in the simplest thermal ALD processes that are the ones used also in the present work (TiO_2, ZrO_2), the first precursor flowing through the reactor is usually the metal precursor e.g., $TiCl_4$, $ZrCl_4$ [75], or another appropriate metal compound [76]. The chemisorption ensures that precursor molecules attach to a limited number of available nucleation sites, usually native OH groups that are already attached to the substrate surface. The amount of adsorbed precursor molecules is limited by the receiving capability of adsorption sites on the surface, so that excessive precursor molecules that cannot be adsorbed on the surface will be removed from the reactor by the flow of inert gas. Hence, ALD exploits the chemical self-limitation and, as a rule, only sub-monomolecular layers can be formed in one reaction step. Before the next precursor pulse there is a delay, usually referred to as a purge period. During this period the carrier gas carries out the gaseous reaction products along with the unreacted precursor. The purge can also be ensured by vacuum, provided that the background pressure is significantly below 10^{-3} Pa inside the reactor. However, in this case relatively long purge periods are needed. The purge is followed by the pulse of the second precursor flow and, after that, by another purge period. This kind of ALD cycle is repeated until the thin film with desired thickness is achieved. As the growth per cycle (GPC) is very small, usually ranging from 0.04 to 0.2 nm in these ALD processes [73], the number of ALD cycles is a parameter allowing precise (and digital) thickness control of the film thickness.

Deposition of TiO_2 by ALD from $TiCl_4$ and H_2O [77] is a typical example of the simplest ALD process. In this case, the overall reaction, described by the chemical formula $TiCl_4 + 2H_2O \rightarrow TiO_2 + 4HCl$, proceeds through the chemisorption of $TiCl_4$ in the first reaction step and reaction of H_2O with surface species in the second reaction step. During the $TiCl_4$ chemisorption $TiCl_x$ ($x < 4$) surface species are formed in the reaction between surface OH groups and $TiCl_4$ while the following purge period ensures removal of HCl formed in this surface reaction and the excess of $TiCl_4$. During the H_2O pulse the Cl ligands of $TiCl_x$ ($x < 4$) attached to the surface during the $TiCl_4$ pulse are replaced by the oxygen atoms and/or OH groups. After the H_2O pulse, another purge is needed to remove HCl as a gaseous reaction product and the excess of H_2O vapor. The OH groups, left

on the surface after the purge, act as nucleation centers during the following $TiCl_4$ pulse, starting the next ALD cycle.

Although ALD is a self-limited deposition method, the exact characterization of the films becomes important not only for the determination of the chemical and phase composition but also for the specification of growth rate as the latter does not have to be a constant parameter throughout the film growth. Generally, in the beginning of the deposition process, when the target compound must nucleate and grow on a substrate with a composition that differs from that of the growing film, the growth rate can be lower as well as higher than the growth rate determined for the film with the stabilized composition and structure [78].

These nuances are emphasized because ALD is generally considered as a thin film deposition method of the finest quality that offers precise thickness control, uniformity and excellent conformity of ultra-thin solid films [70,72,74,79]. Nevertheless, for the deposition of any novel material, the ALD process parameters, for instance, partial pressures and pulse durations of precursors as well as the substrate temperature affecting the phase composition and purity of the film material must be established in the experiments where the process parameters are varied and optimized to deposit thin films with the properties that fit with the theoretical design goals. Despite this kind of optimization, minor amounts of structure and composition defects, which may become important in engineering RS media, are not totally avoidable even in the films deposited by this method.

1.2.2 Chemical vapor deposition

Chemical vapor deposition (CVD) is a general thin-film deposition method based on chemical reactions of gaseous precursors with each other and/or with a solid surface. In the classical CVD, all precursors needed for the synthesis of the film material are directed to the reaction chamber simultaneously. As a rule, carrier gas flow is used to carry the precursors to the substrates. The CVD processes have most frequently been performed at normal or reduced gas pressures. To stimulate the chemical reactions and control the phase composition, the reactor and/or substrates are heated to elevated temperatures in accordance with precursor chemistry considering, for instance, the decomposition and evaporation temperatures of the precursors as well as those of the film material obtained.

In the case of CVD, the film growth significantly depends on the deposition temperature, reaction kinetics and mass transport. Therefore, the thicknesses of films grown by CVD considerably depend on the substrate temperature, partial pressures of precursors, carrier gas flow, and duration of the deposition process. However, if these process parameters are precisely and reliably controlled, and a reactor with an appropriate configuration allowing uniform distribution of precursors on large-area substrates is used, homogenous thin films can be grown by CVD with high deposition rates yielding high throughput and low process cost [80]. For these reasons, CVD is industrially used for large-scale fabrication. For example, development and production of solar panels but also deposition of various functional coatings can be mentioned in this connection [81]. However,

when considering the properties and quality of the thin solid films at technology node <100 nm the uniformity and conformity of CVD metal-oxide thin films is lower compared to those of the ALD thin films [79].

Nevertheless, CVD has found extensive application in synthesis of two-dimensional (2D) materials. After successful exfoliation of graphene in 2004, the interest in the 2D materials as well as in the alternative fabrication methods of these materials was awoken [82,83]. It has been demonstrated in the corresponding studies that 2D materials such as graphene and hexagonal boron nitride (hBN) can be grown by CVD [83]. For instance, these materials can be grown epitaxially on Cu, Ni, and Pt, which promote the formation of crystal structure defining the 2D material [84]. High quality graphene is usually grown at temperatures around 1000 °C with conventional CVD, whereas scientists are developing ways to prepare graphene at temperatures below 600 °C [85].

To apply a 2D material synthesized in this way in the combinations with other materials, the 2D material grown on Cu, Ni, or Pt is later separated from the initial substrate and transferred onto a target substrate [86]. However, the preparation remains challenging due to the high temperatures necessary for the formation of 2D materials by CVD and defects induced by the transfer process [87,88]. Therefore, in more detail, the synthesis, transfer, properties, and application of graphene used in earlier studies related to the topic of this thesis will be discussed in Section 1.4.5. In the present thesis work, graphene layers were synthesized by CVD and transferred onto SiO_2 dielectrics via a wet transfer procedure to engineer HfO_2-graphene-SiO_2-based RS media [**III**].

1.2.3 Electron beam evaporation

The deposition of various metal electrodes (Ti, Au, Pt, etc.) for different electronic devices can successfully be carried out by electron beam evaporation (EBE) method. EBE is a physical vapor deposition method, considerably differing from the previously described ALD and CVD. The EBE processes are conducted in high-vacuum chambers usually pumped down to pressures of 10^{-4}–10^{-8} Pa. High energy of electron beam is used to heat up and evaporate the metals during deposition of the electrodes for RS MIM structures. The high vacuum in the evaporation chamber ensures that the mean free path of evaporated atoms or molecules exceeds the distance between the sample and electrode metal source heated by the electron beam. In this case, the evaporated material can easily reach the sample surface and condensate on that, forming an electrode layer. An advantage of EBE compared to other vacuum evaporation methods is that materials with very high evaporation temperatures (e.g., Ti and Pt with evaporation temperatures exceeding 1500 °C) can be deposited.

To define the shapes of the electrodes deposited by EBE, a physical shadow mask of electrode matrix is usually placed on the top of a sample. However, when electrode sizes are smaller than few tens of micrometers, for instance, when the crossbar design of electrodes is the target, then lithography methods are usually applied for the patterning of the electrodes deposited by EBE. In the fabrication

of RS structures studied in this work, the EBE method was used for the deposition of Pt contact layers on bottom electrodes (BE) as well as Pt, Ti, Au or Ti/Au top electrodes (TE). In some experiments EBE was combined with the lithography methods to pattern the electrodes. In addition, EBE was used in separate experiments to grow SiO_2 films directly onto graphene.

1.2.4 Thermal annealing

Thermal annealing is a generally known heat-treatment procedure employed to modify the properties of various materials. Additional energy given to a material during its heating allows rearrangement of atoms to achieve the lowest energy states in the material, stronger chemical bonds, and higher stability against external influences. For instance, annealing at sufficiently high temperatures enables the amorphous material to achieve higher densities and/or crystallize [89]. In addition, crystalline phases initially formed in the thin films can be transformed to more stable ones as a result of the annealing processes [90]. Consequently, many properties of thin films, such as electrical, mechanical, optical parameters could be changed by annealing dependently on the temperatures and environments used.

Annealing is also applied to purify the thin-film materials. In this case, the choice of environment, usually a gaseous one, is of particular importance. Chemically inert environments, for instance argon gas or high vacuum, reduce the probability for undesirable composition changes while chemically more active gases, e.g. hydrogen and oxygen, can help to passivate or remove unwanted impurities and structure defects. For example, Duenas *et al*. [91] revealed marked decrease in the impurity concentration of TiO_2 films deposited by magnetron sputtering as a result of annealing at 900 °C in the oxygen environment. Hudec *et al*. [92] have demonstrated that annealing in the flow of oxygen reduced leakage currents in the TiO_2 based MIM structures [92]. Chen *et al*. [60] mentioned that thermal annealing of HfO_2 in H_2 of NH_3 enhanced bipolar resistive switching stability in this material. Based on these results, the thermal annealing was also used for the treatment of some RS media described in this thesis.

1.2.5 Optical maskless lithography

Lithography process is one of the most relevant micro and nanoscale technologies in fabrication of integrated circuits (IC) [93,94]. Since the beginning of the era of monolithic ICs, lithography process enabled preparing contact traces between multiple devices on the same chip, eliminating the need for bulky electrical contacts for connecting single devices that were previously prepared separately. Even more importantly, lithography is also used to achieve precise doping of specific regions of the semiconductor to achieve desired electrical properties [94]. Notably, nowadays the printed circuit boards (PCBs) are also produced in similar lithography processes.

Traditionally an image that determines 2D physical shape of wanted features/ patterns on a sample surface is transferred to the resist layer exposing the resist

to light or another radiation through a mask attached to the sample that is being processed. The resist itself is typically a specific polymer layer that is usually spin-coated onto the sample surface. As a result of the exposure, some properties of unmasked resist are modified. Depending on whether a positive or negative resist is used, the resist can be selectively removed from the area that was exposed or not exposed, respectively, to the radiation. After this lithography step, the areas of the sample uncovered by the resist are ready for the following treatment, e.g. etching, doping or deposition of electrical contact material.

The main principles of photolithography apply also in the case of optical maskless lithography (OML) used for preparation of electrodes with different shapes, sizes, and/or configurations in certain experiments of this study to configure titanium top electrodes. However, differently from the conventional microscale photolithography, where contact or proximity shadow masks are used, no physical mask is needed in OML. Instead, UV or deep UV ($\lambda \approx 0.2–0.4$ μm) laser or light-emitting diode beam operated by a spatial light modulator (SLM) matrix [93] is used to generate the image of the pattern on the sample surface. The SLM matrix consists of arrays of micromirrors (with single mirror size of around 10×10 μm^2). The orientation of micromirrors can be controlled by the electric field while the laser or light-emitting diode beam is correspondingly modulated to obtain a required image of features in the photoresist. Hence, the SML matrix replaces conventional physical mask [93]. This enables faster computer-aided design (CAD) of lithography processes, as the fabrication of high-precision and expensive physical masks is not needed. In any case, the lithography processes must be conducted in a very clean environment, i.e., in a clean room, because otherwise dust particles settling on the sample can cause defects in the lithographed structures. For the same reason, other lithography-related processes (sample cleaning, photoresist coating etc.), which are critical towards the dust contamination, are also carried out in the cleanroom. The application areas of OML range from microelectromechanical systems (MEMS) to microelectronics and precision optics [95,96]. However, in the nanoscale lithography, focused ion or electron beam has to be used [96].

1.3 Methods for characterization of resistive-switching media

The most important for this thesis was the electrical characterization of samples to investigate RS properties such as switching voltages and currents, endurance, and memory state retention. However, the RS media deposited for corresponding MIM structures studied in this work were characterized firsthand using several methods commonly employed for investigating the physical and chemical properties of thin films. The elemental and chemical compositions were investigated by X-ray fluorescence spectroscopy (XRF) and X-ray photoelectron spectroscopy (XPS). The phase composition was determined by X-ray diffraction analysis (XRD). High resolution scanning electron microscopy (SEM) was used to study

the surface morphology. Cross sections of RS structures were characterized by transmission electron microscopy (TEM) was applied to assess the structure, quality and chemical composition of the multilayer structures. The main principles of these characterization methods are briefly described in the following sections of the thesis. However, most important for this thesis was the electrical characterization of samples to investigate RS properties such as switching voltages and currents, endurance, and memory state retention.

1.3.1 X-ray fluorescence and X-ray photoelectron spectroscopy

X-ray fluorescent spectroscopy (XRF) is a quantitative characterization method to evaluate presence and amounts of chemical elements in solids. The working principle of XRF is based on fluorescence, i.e., fast response (<1 s) of luminescence, excited by X-rays. For excitation of fluorescence, high energy X-rays are used to excite electrons out of low-energy electron states of atoms that form the solid. The empty electron states are filled by electrons from electronic states with higher energies to restore the stability of the atoms. The latter process is called electron relaxation. Energy is being released in this process in the form of photons, which usually have lower energy and, hence, higher wavelength than the photons used for excitation. Each chemical element, having at least 2 electronic states in its atoms, has intrinsic emitted photon wavelengths/energies dictated by the electronic structure of the atoms [97]. Therefore, recording the emission wavelengths and intensities, the presence of chemical elements can be detected and the concentrations of those can be estimated from the XRF data. The information depth of the XRF analysis, that is, the thickness of the surface layer yielding reliable information about the composition, depends on the material studied. For the materials studied in this work, the information depth is a few micrometers, whereas the functional oxide films were grown to thicknesses ranging from 10 to 50 nm. Therefore, X-rays penetrate these films and the XRF method yields information about composition with appreciably high accuracy [98].

To perform more detailed composition analysis, including characterization of the electronic structure, chemical bonds, and presence of functional groups (oxides, hydroxides), a more sophisticated method, X-ray photoelectron spectrometry (XPS) should be employed. In the XPS analysis, a sample is excited with a monochromatic X-ray with known photon energy. As a result, electrons are ejected from the electron shells of atoms present in the sample. If the photon energy is sufficient, the electron becomes a ballistic photoelectron. However, the kinetic energy of emitted electron is lower than that of the incident photon, as some of the energy transferred to the electron was required to break the electron-atom bond. After measuring the kinetic energies of emitted ballistic electrons, it is possible to calculate the binding energies from the data obtained. The binding energies of the electrons, corresponding to the intrinsic energy levels of the atoms present in a solid, form a spectrum that is characteristic for each chemical element [99]. Although besides X-rays (λ = 0.01–10 nm), ultraviolet (UV, λ = 10–400 nm) radiation can also be used for generation of photoelectrons. A downside

of XPS is the fact that the photoelectrons generated deep inside the sample cannot escape the sample. Thus, the method is a surface-sensitive analysis method able to analyze the surface layer with a thickness that usually does not exceed 10 nm [100].

1.3.2 X-ray diffraction analysis

X-ray diffraction (XRD) is a method routinely employed for characterization of thin films to define the correspondence of synthesized material to the desired phase composition, crystallinity, and orientations and sizes of crystallites. In a crystalline specimen, the atoms or molecules form a systematically ordered pattern (lattice), which acts as a diffraction grating. In this pattern, there are sets of lattice planes, each of those denoted by Miller indices (h,k,l). In XRD studies, the sample is irradiated by coherent monochromatic X-ray radiation. The radiation reflects from the planes obeying rule of reflection (Figure 3). Hence, the angle between the reflected beam and the plane is equal to the angle (θ) between the incident beam and the plane. Since the distance between neighboring planes (interplanar spacing) in the set of planes is constant, constructive interference occurs at appropriate diffraction angles. The criterion for constructive interference is known as Bragg's law, $n\lambda = 2d_{hkl} \sin\theta$, where n is the order of reflection, d_{hkl} is the interplanar spacing, and λ is the wavelength of the X-ray radiation. Classical configuration (Bragg-Brentano geometry, Figure 3) to collect diffraction pattern is based on moving the detector attached to goniometer and changing the incidence angle of the beam in the manner that the angle between the incident beam and sample surface is varied equally with the angle between the diffracted beam and the sample surface [101,102]. This XRD analysis mode is also denoted as $\theta/2\theta$ or $\theta - 2\theta$ XRD.

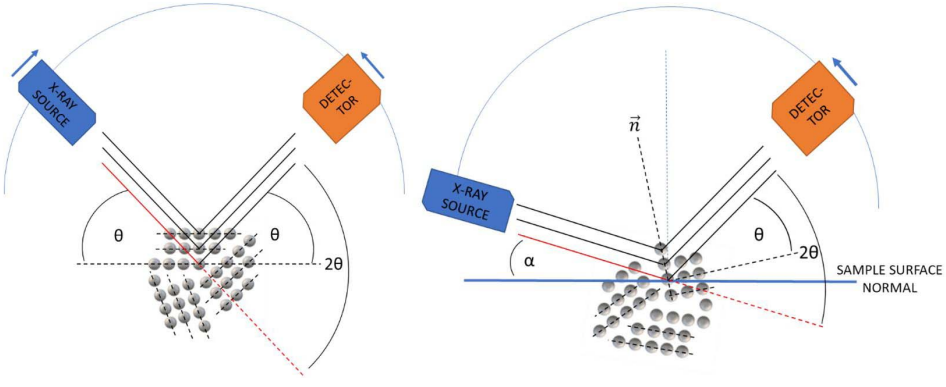

Figure 3. Bragg-Brentano geometry (configuration on the left) compared to GIXRD geometry (configuration on the right), where α is a fixed incident beam angle and $\vec{n}$ is the lattice plane normal.

In the measurements of very thin solid films (<20 nm), the incident beam angles greater than 5° cause large amount of noise because the X-rays start to penetrate deep into the substrate. Hence, grazing incidence X-ray diffraction (GIXRD, Figure 3) geometry is often used by fixing the incident beam at a small angle (<2°) and moving the detector over the 2θ range of interest. Low incident angle increases the X-ray path length in the film material and enables measurement of the diffraction signal from a larger area of the sample [103].

The X-rays applied in XRD studies are generated in a vacuum discharge tube with a heated cathode and cooled anode. Most frequently copper anodes, emitting K_α radiation of Cu with a wavelength of 0.1542 nm (1.542 Å) are used in these tubes. The voltages applied to the X-ray tubes are usually 35–50 kV. The K_α radiation is generated as a result of electron relaxation from the second (L) electron shell to the first (K) electron shell. However, intrinsic K_β lines, caused by the electrons relaxing from the third (M) electron shell to the K shell, are also generated by these tubes. This relaxation of electrons generates radiation with slightly higher energy and lower wavelength (λ = 0.1392 nm) compared to those of K_α lines. The K_β lines also contribute to XRD, making the interpretation and analysis of the XRD patterns more difficult. Therefore, physical filters (monochromators) are used in X-ray diffractometers to dampen the unwanted K_β lines.

All crystalline materials possess characteristic diffraction patterns occurring at intrinsic diffraction angles, often expressed as 2θ with respect to incident beam itself. Therefore, generally recognized reference patterns are often added to the diffractograms in order to simplify the interpretation of results for a reader. For the characterization of RS materials studied in this work, GIXRD was applied because this method is the most convenient one for the characterization of thin films, yielding XRD signal from a large area but also limiting X-ray penetration into the substrate and, hence, increasing the relative reflection intensities of interest [101,102].

1.3.3 Electron microscopy

Electron microscopy is extensively used in the materials science to study the morphology and structure of solid materials with a very high spatial resolution. The era of electron microscopy began in 1927, when C. Davisson and L. Germer [104] demonstrated the wave-like properties of electrons by irradiating crystal with electron beam and obtained ring pattern similar to XRD, i.e., electron diffraction pattern of crystalline structure. The experiment itself, carried out at Bell Labs, is known to the scientific community as the Davisson-Germer experiment. The electron diffraction patterns can be used to characterize the crystal structure of different solid materials with the spatial resolution determined by the sizes of the focused electron beam [105]. As the electron beam can be focused on very small areas, studies with very high resolution can be performed using the electron microscopy methods.

Scanning electron microscopy (SEM) is a method widely used in the materials science to study the morphology, crystal structure, grain sizes and shapes, and

thicknesses of solid thin films. The SEM method is based on the irradiation of a sample with an electron beam. When the electron beam is focused on the sample, secondary electrons generated by the primary electron beam as well as back-scattered or reflected electrons provide the signals that are usually detected by different detectors. The sample is scanned in the directions of X and Y axes and the signals of different detectors are used to construct an image of the sample surface obtained with a spatial resolution down to the sub-nanometer range. As a result, the SEM study gives images of the sample providing information about the topography, composition, and microstructure of the sample.

Transmission electron microscopy (TEM) is another powerful and precise, but expensive method to study interfaces, lattice ordering, and short-range phase composition of different materials, including nanostructures and thin solid films. In the TEM method, electron beam with electron energies high enough to transmit through a sample are used to irradiate a sample and get the information. The transmitting electrons interact with the electronic structure of a specimen and generate an image on the scintillator screen. The actual image of the material structure inside the specimen is generated with the application of wave-matter interaction principles and theory, using quantum-physics related tools [106,107]. The thickness of the samples that can be used in TEM studies should not exceed few micrometers. Therefore, in most cases, the preparation of samples with appropriate sizes is an important part of TEM studies. TEM analysis provides invaluable information about the crystal structure and composition of materials, quality of interfaces between constituent layers in multilayer structures and superlattices, components of chemically heterogeneous nanomaterials, and sizes of nanocrystals and nanolayers. All these studies can be carried out with the 0.1-nm-level or even higher resolution.

1.3.4 Electrical characterization of RS structures

Measurement of electrical characteristics is the most direct and important method for characterization of RS structures to obtain information for correct interpretation of RS processes in different materials. Most important parameters that should be determined in these measurements are U_{SET}, U_{RESET}, and memory window defined as I_{LRS}/I_{HRS} or R_{HRS}/R_{LRS} where R_{HRS} and R_{LRS} are the resistances in HRS and LRS states, respectively. Furthermore, endurance and retention characteristic as well energy consumption and switching speed are the important parameters characterizing the application potential of an RS device. Typical industrial expectations for RRAMs are $I_{LRS}/I_{HRS} \geq 10$, endurance $>10^9$ switching cycles, retention $>10^6$ s (at 85 °C), absolute values of operating voltages <1 V, energy consumption ~10 pJ/transition, and switching time <10 ns/per transition [108].

A common way to start the electrical characterization of RS structures is to measure the I-V curves [38]. These measurements are usually performed sourcing the voltage with defined steps and measuring the currents corresponding to each voltage step. As a rule, the I-V curves are measured sweeping the voltage in both direction, that is, first the absolute value of voltage is increased from zero to a

certain value and then it is lowered back to zero. In most cases, the measurements should be made at both voltage polarities. From the analysis of the I-V loops recorded in these measurements, one can see, if and how much the resistance has changed during the recording of I-V curves in the voltage ranges selected. In order to avoid the irreversible breakdown of the devices, the maximum current through a device should be limited using the current compliance option of the voltage source.

This kind of I-V-curve measurement cycles are also used for electroforming of a RS device, that is, for formation of CF in the RS medium of the device. An abrupt increase in the absolute value of current is the evidence of CF formation. However, often the electroforming procedure is carried out in the current sweeping mode. This means that the DC power supply is configured to define the current that is step-by-step changed from zero to a certain value while the voltage on the RS device is measured for each current step. In this case, a significant decrease in the absolute value of voltage with increasing absolute value of current indicates the CF formation.

The further measurements of the I-V loops depend on the RS type (BRS, URS, CRS), discussed in Section 1.1.2 of this thesis. For these measurements, it is important to find optimal voltage sweep ranges allowing switching the device to HRS at U_{RESET} as well as to LRS at U_{SET}. It has to be noted in this connection that the absolute value of U_{SET} needed to recover CF after its disruption is usually lower than the absolute value of the voltage needed for initial formation of CF. Additionally, during switching to LRS it is necessary to apply appropriate current compliance because in the case of the most RS media, the I_{LRS} and I_{HRS} values may markedly depend on the current compliance levels.

Form the I-V-loops recorded at the optimized measurement parameters, U_{SET}, U_{RESET}, I_{LRS}, and I_{HRS} can be determined, while I_{LRS} and I_{HRS} are determined at a voltage U_{READ} that is usually chosen from the range extending from –0.3 to 0.3 V [11,38,109].

In the most basic configuration of the I-V measurements, the voltage is varied in the linear manner. This means that in the time scale, the applied voltage has a triangular shape [110]. However, if it is necessary to minimize the current-voltage stress, the pulsed signal can be applied as well. If a pulse signal generator is used, it is possible to control the pulse durations even more precisely than with SMU and apply different pulse shapes, e.g. ramping the voltage pulse from zero to each sequential voltage point [111]. Timing the pulses gives a better control over a plausible current overshoot [110].

Besides the measurement of parameters that can be determined from an I-V loop, there are two important types of electrical measurements, called endurance and retention measurements. The endurance measurement is a cyclic test. The device is repeatedly switched from HRS to LRS and from LRS to HRS, and the current (or resistance) is measured at U_{READ} after each switching procedure. This measurement resembles the realistic application of RRAM. The endurance characteristic is expressed as the dependence of I_{LRS} and I_{HRS} (or U_{LRS} and U_{HRS}) on the number of switching cycles. The current or resistance values can be

extracted from the I-V loops but more commonly this measurement is carried out by applying a series of voltage pulses U_{SET}, U_{READ}, U_{RESET}, and U_{READ} in each endurance measurement cycle and measuring the current or resistance during each U_{READ} pulse. In the latter RS endurance measurement mode, appropriate choice of the state-writing pulses is also important, especially because SET and RESET may require different switching pulse durations [112]. Timing constraints can be identified by determining the time required for each transition as a function of the pulse amplitude [113]. The data that are obtained for the SET or RESET pulse duration (t_{SET}/t_{RESET}), current (I_{SET}/I_{RESET}) and voltage (U_{SET}/U_{RESET}), needed for switching the device from one state to another one, enables one to calculate another important electrical parameter, that is, operation energy per bit, which is in principle expressed as $E = U \times I \times t$ [20]. The maximum RS switching speed is also a crucial parameter of an electronic memory device. The measurement can be conducted using pulse generator, oscilloscope and external current limiting circuitry [38]. The pulses are applied to the device to switch between the states while the oscilloscope enables one to evaluate the time required for each transition. Current limiting circuitry is used to avoid irreversible dielectric breakdown.

The RS state retention measurements are made to determine the nonvolatility of the resistance states. The results are recorded and expressed as persistence of either low or high resistivity state value in time. The device is switched to one of the states either by applying writing pulse or conducting I-V loop measurement and the state is measured by applying reading pulses over a period of time sufficient for determination of considerable changes in the current or resistance of the state. Although there are no agreed conditions of retention measurements, the duration of retention measurements in different publications is often around 3 to 6 hours [114–119]. Nevertheless there are also a lot of studies where retention characteristics have been measured during >200 h [120–124]. Retention measurements have been carried out at room temperature [115,125,126] as well as at temperatures elevated up to 250 °C [121,122]. The retention measurements conducted at higher temperatures enabled the researchers to reduce the time needed for these studies. The retention measurements, conducted at higher temperatures, together with extrapolation methods are usually used to calculate room-temperature retention times extending to very long periods (up to 5–10 years as can be found in the literature [127,128]).

Thorough electrical measurements also require evaluation of the device-to-device repeatability, in other words, contact yield. This is the most time-consuming process, that cannot be omitted. Nevertheless, it is important to note that in the early-stage studies of a new RS medium, statistical analysis can be less comprehensive as there are several ways to further optimize the RS performance, for instance, changing the material deposition and post-deposition heat treatment process parameters. However, for evaluation of industrial producibility, thorough statistical analysis of all the crucial parameters must be made.

1.4 TiO_2, Al_2O_3, ZrO_2, HfO_2 and graphene as RS materials

Around the world, RS initialization and properties have been investigated in various materials (metal oxides, chalcogenides, polymers, carbon-based materials) and their combinations. In a recent publication, Asif and Kumar [129] give comprehensive overview of RS materials including interesting aspects of neuromorphic computing. The focus of the present thesis is on characterization of RS in structures tailored from industrially acknowledged high-k metal oxides (Al_2O_3, HfO_2, ZrO_2, TiO_2) earlier applied as dielectric in DRAM structures(Al_2O_3, ZrO_2) or gate dielectrics in processor transistors (HfO_2).

Al_2O_3 was probably the first wide-bandgap high-k metal oxide applied as a capacitor dielectric, replacing low-permittivity SiO_2 in DRAM cells. In order to accommodate functional Al_2O_3 layers with contemporary three-dimensional architecture of trench capacitors [130], atomic layer deposition technique became the natural choice upon high volume production of chips. Thereafter, search for even higher permittivity oxides was initiated to further increase memory bit densities.

Since 2007 [73,131] HfO_2 films grown by ALD have been applied as high-permittivity gate dielectrics of field-effect transistors (FETs) that can be used in central processing units (CPU) of computers. However, HfO_2 as a DRAM dielectric was replaced by ZrO_2 [132]. Differently from HfO_2, which predominantly crystallizes in the stable monoclinic phase ($k < 30$), very thin ZrO_2 films tend to crystallize in the cubic and/or tetragonal phase ($k \approx 37–47$) [133]. In order to further improve the performance of DRAM, stacks of $ZrO_2/Al_2O_3/ZrO_2$ films [134–137] as capacitor dielectrics were accommodated with chip production lines. The application of amorphous Al_2O_3 between nanocrystalline ZrO_2 layers was necessary, to firmly stabilize the desired polymorphs of ZrO_2 and reduce the leakage currents in DRAM cells.

Rutile phase of TiO_2 has been one of the potential high-k dielectrics of the next generation DRAMs. Owing to its superior permittivity ($k \approx 100$), it has been studied extensively for a long time [133,138]. Unfortunately, TiO_2 has rather high leakage currents due to its relatively narrow bandgap (3.0–3.4 eV). Thus, doping of TiO_2 with Al and application of multilayer stacks, containing Al_2O_3 layers in addition to TiO_2 layers, have been investigated to reduce the leakage currents [133,139].

Since the materials listed here have also shown potential for RS applications, the further RS studies of various combinations of these materials was a natural choice of research. To describe the background, the following sections will focus on the earlier investigation of RS in MIM structures where these oxides served as the RS media. Additionally, insight will be given into RS application of 2D materials focusing on graphene that was also studied in this thesis work.

1.4.1 Al_2O_3

Besides the application of Al_2O_3 as a dielectric in volatile DRAM capacitors, interest in Al_2O_3 as a solid medium potentially suitable for non-volatile storage of bits appeared. In one of the earliest studies of RS in Ti/Al_2O_3/Pt structures, Lin *et al*. [140] demonstrated BRS with the HRS/LRS ratio of 10^3 and possibility to use short (10 ns) writing pulses. Moreover, RS was obtained even at a temperature as high as 150 °C. The same authors also revealed that systematic thermal annealing led to a decrease in the initial forming voltage and increase in the SET voltage [141]. A more recent study of Ryu and Kim [142] demonstrated bipolar and unipolar resistive switching in the Cu/Al_2O_3/Si structure with a 3.5 nm thick Al_2O_3 layer yielding HRS/LRS ratio of 10^5. Sarkar *et al*. [143] reported that dividing the initial formation into several steps by applying increasing current compliance, resulted in the gradual RESET leading to multi-state RS in Pt/Al_2O_3/Ni devices. According to the results of Wu *et al*. [144], different top electrodes can evoke either unipolar or bipolar RS in MIM structures with the Al_2O_3 dielectric. Huang *et al.* [145] have demonstrated forming free RS with fast operation speed (28 ns), large HRS/LRS ratio (10^3) and high endurance (10^{10}) in W/AlO_x/Al_2O_3/Pt structures. Additionally, owing to its good dielectric properties Al_2O_3 has been often used as a component layer of multi-layer RS structures enabling to enhance RS parameters [68,146,147]. For example, Mahata *et al*. [148] demonstrated gradual RESET and remarkable multi-state RS in TaN/HfO_2/Al_2O_3/HfO_2/ITO structures. It has been suggested that Al_2O_3 layer with relatively low permittivity combined with high-k materials, may accommodate the rupture and reformation of CF relevant to multi-state performance [149].

1.4.2 TiO_2

Titanium oxides with variable stoichiometry belong to a group of transition metal oxides. Within the last two decades a number of studies, devoted to resistive switching in structures containing titanium oxide layers with different stoichiometry and/or crystalline structure, have been published. The main crystalline polymorphs of TiO_2 are anatase, rutile and brookite. In addition, titanium oxide can form several Magneli phases while some of these phases can be highly conductive. This makes TiO_2 attractive for RS applications. For instance, Kim *et al.* [62] have demonstrated high transmission electron microscopy images of conductive filaments in anatase-phase TiO_2, where the filament phases were determined to be Ti_4O_7 and Ti_5O_9 in the Pt/TiO_2/Pt structures. The phase change phenomena in TiO_2 can be classified as oxide bulk limited process caused by VCM [149]. Kleiman *et al*. [150] revealed that devices with rutile- and anatase-phase TiO_2 dielectrics showed higher resistance in HRS, whereas devices with amorphous TiO_2 were generally more conductive. Furthermore, Kim *et al*. [62] also demonstrated that one of the main problems related to endurance characteristics of such devices with symmetric electrodes is the localized decrease in

concentration of oxygen ions in the proximity of CFs due to repeated RS processes at one polarity. Thus the oxygen vacancy or ion drift and diffusion somewhat largely affect conductivity of the bulk oxide and electrode or constituent layer interfaces [149]. For example in the same study by Kleiman *et al*. [150] Pt top and Ti bottom electrodes were used in case of both crystalline and amorphous TiO_2 RS layer, but the active region of RS was suggested to be Pt-TiO_2 and TiO_2-Ti respectively. The concentration of oxygen vacancies at the Pt-TiO_2 interface can also control the height and width of Schottky barrier caused by the difference in the work functions of the metal electrode and oxide [149,151]. However, electrode combinations with chemically active metal such as Ag or Cu complicates the RS mechanism even further as ECM can become involved. For example, Jena *et al*. [152] demonstrated that Ag/TiO_2/Pt BRS artificial synapses can mimic Pavlov's associative learning. Sahu *et al*. [153] studied the origins of resistive and capacitive contribution affecting the RS processes in Cu/TiO_2/Pt structures and concluded that the effect of filamentary RS on the capacitance is negligible. Relatively high conductivity of TiO_2 films may complicate the stabilization of RS behavior and control over the switching stability, but the oxide may become applied in combination with highly insulating ones, such as Al_2O_3, allowing one to tailor superior properties of different materials.

1.4.3 ZrO_2

Zirconium dioxide (ZrO_2), also known as zirconia, has been considered as an appropriately defective (in terms of oxygen vacancies) solid medium for non-volatile RS devices [154]. Thus, zirconia as a transition metal oxide has been a natural choice to be studied as a possible RS medium. Theoretically, potential influence of different dopant elements (e.g., Ti, Y, Mo) on RS in ZrO_2 has also been studied [155], without consideration of Al, though. It seems that a paper by Pan *et al*. [156], reporting of reliable multi-state RS in yttria stabilized zirconia (YSZ) in the Cu/YSZ/Au structures in 2012, brought more serious interest to zirconia as a RS medium, although even earlier studies by Guan *et al*. [157] and Lin *et al*. [158] demonstrated already in 2007 that RS can be obtained in ZrO_2 combined with gold nanocrystals in Au/ZrO_2-nc-Au/Si(doped) structures and in Ti/ZrO_2/Pt structures. More recent publication of Abbas *et al*. [154] has reported that rapid thermal annealing in an oxygen environment can precisely control the content of oxygen vacancies in zirconia of Ti/ZrO_x/Pt structures and, hence, modify the RS parameters inferring the imperative role of oxygen vacancies. Lee *et al*. [159] introduced a low-cost and low-temperature method for production of zirconia based RS structures by applying UV treatment and attesting that longer UV treatment can enhance the RS stability. Thus, the ZrO_2 is a promising material to be used in RS devices those RS can be easily tuned by controlling the content of oxygen vacancies through the thermal annealing process technology.

1.4.4 HfO_2

Since the discovery of ferroelectric properties of hafnia (HfO_2) crystallized in the orthorhombic phase [160], HfO_2 has also been investigated as a material relevant to the nonvolatile memory technology. Since then, HfO_2 as the "heart" of ferroelectric field effect transistors, FeFET's, has been advertised [131]. However, a significant number of studies have also been devoted to the characterization of HfO_2 as a RS medium. HfO_2-based RS devices have demonstrated some of the best performances from the reproducibility and endurance perspective [27].

Vinuesa *et al*. [37] have investigated, how the thickness of hafnia could influence the BRS direction in Pt/HfO_2/Ti structures. Kim *et al*. [161] further studied the thickness effects and revealed that the Cu/HfO_2/Pt structures with thinner HfO_2 dielectrics demonstrated gradual RS while samples with thicker HfO_2 yielded more abrupt RS. Yuan *et al*. [59] reported that nitridation treatment enhanced RS endurance in Pt/HfO_2/TiN structures. Napolean *et al*. [162] have published a thorough review on RS in structures containing HfO_2. Milo *et al*. [163] studied multi-state RS in TiN/HfO_x/Ti and TiN/HfAlO/Ti structures and concluded that amorphous HfAlO showed superior performance compared to amorphous and poly-crystalline hafnia used RS structures for neuromorphic processing. Furthermore, Lan *et al*. [164] demonstrated that neuromorphic devices with Ti and Pt electrodes and Zn-doped HfO_2 dielectrics can show up to 90% accuracy of results. Kim and Yoon embedded HfO_2 based RS layer into field effect transistor as a neuromorphic synapse transistor with improved energy consumption and operational stability [69]. One can also realize that the number of studies wherein HfO_2 is combined with other oxides, dopants, nanodots etc. is markedly high [165–169]. Owing to its applications in electronic industry as a gate dielectric, HfO_2 may belong to the metal oxides that are also most intensely studied as a resistive-switching dielectric.

1.4.5 Graphene

Various 2D materials such as graphene, graphene oxide, transition metal dichalcogenides (TMDs) have demonstrated interesting electrical properties and for this reason, can act as transparent and flexible electrodes, dielectric materials and also RS materials or constituents of RS devices [170–172]. One of the earliest reports on RS in structures containing graphene was published in 2008 and described planar FET with graphene- and graphene-oxide-based channel exhibiting non-volatile resistance change of the channel up to six orders of magnitude that can be switched between conductive and less conductive state by sweeping voltage on the gate electrode [173]. URS with HRS/LRS ratio of 10^6 and endurance of 10^3 cycles has been demonstrated in planar graphene nanoribbons with approximately 0.2 μm width placed between two Pt electrodes with 0.5 μm spacing [174]. Shindome *et al.* [175] studied graphene nanoribbons of similar sizes between the Cr and Ti electrodes. They concluded that URS taking place was independent of the electrode material. Lee *et al.* [176] reported that

Pt/graphene/NiO/Pt devices, exhibiting URS, demonstrated lower variance of U_{SET}, U_{RESET}, and resistances in HRS and LRS than the Pt/NiO/Pt devices did. They concluded that modest concentration of additional defects related to presence of graphene in the structure enabled better control of the CFs in the structure. Zhao *et al.* [123] showed that a nanohole in graphene layer determined the position of CF formed by ECM in an Ag/graphene/SiO_2/Pt device exhibiting BRS. The endurance of the device reached $>10^7$ RS cycles. Zhang *et al.* [177] demonstrated a highly compact combined RS transistor with graphene electrodes, WS_2 (TMD) channel, and hBN gate dielectric acting simultaneously as an RS layer between the channel and drain electrode.

1.4.6 Concluding remarks on previous RS studies

There is an enormous number of publications dedicated to different RS structures as well as materials and their combinations applicable in RS devices. Promising results have also been obtained for RS structures based on TiO_2, Al_2O_3, ZrO_2, HfO_2, and graphene that the research described in this thesis is based on.

Table 2. Comparison of different RS structures.

RS media deposition technique	TE	RS media	BE	HRS/ LRS ratio	Endur-ance, cycles	Reten-tion, s	U_{SET}, V	U_{RESET}, V	Ref.
RF Sputtering /ALD	W	AlO_x/Al_2O_3	Pt	10^3	10^{10}	10^6 s	1.05 V	–1.3 V	[129]
ALD	Ta	HfO_2	Pt	<10	10^{11}	$>10^6$ s	1.3 V	–3 V	[63]
ALD	Pt	HfO_2	TiN	$>10^3$	$>10^2$	10^4 s	2 V	–2 V	[63]
RF Sputtering	Pt	ZrO_2	TiN	~10	10^4	10^3 s	0.8 V	0.5 V	[178]
RF Sputtering	Al	Al_2O_3/ZrO_2	Al	10^2	10^2	10^5 s	–4 V	1.5 V	[179]
ALD	Pt	TiO_2	Ru	10^3	10^2	10^6 s	2 V	1V	[180]
PEALD	Al	$TiO_2/Al/TiO_2$	Al	>10	10^4	10^4 s	–2.5 V	2.5 V	[180]

Nevertheless, it is obvious that significant additional studies are needed for the development of RS devices and technologies suitable for wide-scale industrial application of RRAM-s.

One problem is that the results obtained so far scatter markedly and cannot always be directly compared to each other as many studies contain preliminary results and/or the characterization process parameters vary from paper to paper, thus not allowing one to reveal the full potential of a certain RS material. Additionally, it is quite common that improving one or few RS parameters leads to degradation in other parameters. It should be emphasized that a general issue is the inherent stochasticity of formation and rupture of CF which gives a rise to important problems concerning large scale production and application. For example, the device-to-device variability in the memory window or resistance in LRS or HRS complicates the electronic and algorithmic controlling of the

memory device containing a large amount of such memristors. Furthermore, stochastic behavior is also present in cycle-to-cycle operation of a single memristor.

Emerging concepts of computing in memory may create additional requirements for electronic memories where RRAM could find its superior application. An important nuance connecting neural networks and RS devices is that RS device does not only retain the resistance state, but it also "remembers" the previous operation(s) as the outcome of the last operation might affect the next one. For instance, if the RS conditions like voltage, current, and switching pulse duration are kept at constant values but, because of stochastic performance of CF, yield different resulting resistance in consecutive RS cycles, the resistance attained always affects the result of the next operation as well. Thus, studying RS in different material combinations which enable better control of RS performance more precisely remains of high interest.

2. OBJECTIVES

In search of commercially usable RS memory structures, a wide range of materials that exhibit RS properties need comprehensive research to fully unlock the potential and achieve mature state of RS technology. As RS can be attained even in material with thickness below 1 nm [149] whereas the mechanisms at that scale are not completely understood, it is very important to be able to precisely control the thickness, conformity and uniformity of constituent layers forming the RS structure. to explore and deeper understand the underlying phenomena. Hence, the investigation of possibilities for engineering RS media in the processes allowing control of the material synthesis at an atomic layer level is of significant scientific interest and practical importance. The ability to engineer materials with sub-nanometer growth precision in ALD processes was expected to allow synthesis and investigation of interesting and promising combinations of materials with supreme RS properties.

The first objective of the present study was to synthesize and evaluate physiochemical properties of selected metal oxide thin films and, thereafter, examine the RS performance of different dielectric oxides and their combinations (TiO_2, Al_2O_3, ZrO_2, HfO_2, SiO_2) in detail. Specifically, the effect of atomic layer doping and multilayer design of RS thin films on the switching voltage, HRS/LRS ratio, and durability of the cells was of interest. ALD was therewith purposefully applied as a method allowing one to conveniently tailor materials of different conductivity and structure for novel RS media with superior properties. The purpose of the studies was engineering of tailored materials, which would potentially enable tuning of RS state currents in order to reduce the power consumption and widen the memory window, thus improving the overall performance of RS memory cells. The main goal of the conducted electrical measurements was to collect information to demonstrate the potential of different RS media.

The second objective of the work was also to demonstrate that ALD-grown thin solid films can be combined with 2D materials, prepared by technologies differing from ALD to exploit novel materials and physical forms, such as graphene, demonstrating the compatibility of ALD with other advanced processes. In particular, the application of graphene, embedded in ALD-grown oxides, was of marked interest in order to establish its influence on switching behavior.

All in all, the thesis is targeted on enhancement of understanding how the design and tailoring of thin-film structures can influence the RS properties of these kinds of novel nanomaterials that may be of significant interest for the engineering community. To achieve this goal, the thesis investigates the use of dielectric materials, extensively studied for their suitability as CMOS and DRAM dielectrics, in new combinations as RS media. Finding new RS structures composed of materials that have been more familiar to semiconductor industry may also enable the industry to utilize fabrication methods that are already in use. The expected results were believed to enrich the scientific knowledge on RS processes and media, and pave the road for further development and application of scientific findings of this field.

3. EXPERIMENTAL METHODS

3.1 Preparation of RRAM structures

The samples studied were MIM structures, deposited on approximately 1 cm × 1 cm substrates cut out of Si(100) wafers. The first layer that was deposited on the Si substrates was the bottom electrode. Rutile-phase RuO_2 [**I**] that promoted the epitaxial growth of the TiO_2-based RS medium in the rutile phase [137,**I**] or titanium nitride (TiN) [**II**,**III**] acted as the bottom electrodes in the studied samples. In all RS structures studied in this work, a bottom electrode was common for all RS cells formed on one substrate. In order to ensure reliable electrical contact to the bottom RuO_2 electrode, a rectangular Pt pad was deposited by EBE on the RuO_2 layer at one edge of a sample (Figure 4, left panel) using a VS-17 (Vacuumservice OY) EBE equipment.

The substrates with TiN bottom electrodes were cut from a commercially-produced wafer with 10 nm TiN layer deposited at Fraunhofer IPMS-CNT (Dresden, Germany) on the boron-doped Si(100) with a resistivity of 0.014–0.020 Ωcm [II]. The electrical contact to these substrates could be established from the back side of a substrate. To improve the electrical contact between the conductive substrate and a probe of a device used for electrical measurements, an Al layer was deposited by EBE on the back side of the TiN/Si(100) substrate (Figure 4, right panel). Prior to the Al deposition the native SiO_2 was etched with 10% HF and water solution.

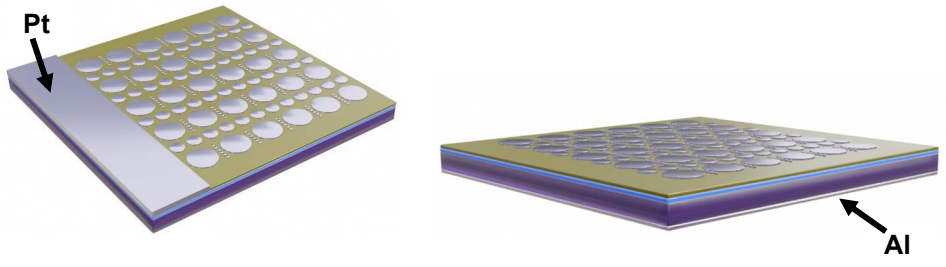

Figure 4. RS structures with circular top electrodes with diameters of 50 µm, 250 µm and 500 µm. The samples with RuO_2 bottom electrodes (left panel) had rectangular Pt contact pads deposited on RuO_2 bottom electrodes at one edge of a sample. The samples with TiN bottom electrodes (right panel) deposited on electrically conductive Si substrates had Al contact layer on the backside of the substrate.

The insulator layers, serving as the RS media in the MIM structures studied in this work, were deposited on the bottom electrodes using a home-made flow type ALD reactor [**I**–**III**] and Picosun^{TM} R-200 Advanced ALD system [**III**].

In the first study the TiO_2-$Ti_xAl_{1-x}O_y$ structures were deposited by ALD at temperature of 350 °C using $TiCl_4$ and $Al(CH_3)_3$ as the Ti and Al precursors, respectively, and H_2O vapor as the oxidizer [**I**]. The main component of this RS medium was TiO_2, which was deposited using the conventional "precursor

followed by oxidizer" ALD cycles. The $Ti_xAl_{1-x}O_y$ layers that were used to modify the RS media were deposited using an unconventional ALD cycle sequence, where consecutive Ti and Al precursor pulses were followed by a H_2O pulse. Each structure was deposited in one ALD process. In one set of samples, TiO_2 was atomic-layer-doped with $Ti_xAl_{1-x}O_y$ using a single ALD cycle for deposition of each dopant layer whereas the dopant layers were evenly distributed throughout the dielectric [**I**]. In another sample set, each sample contained a single $Ti_xAl_{1-x}O_y$ layer deposited with 1–6 ALD cycles between two TiO_2 layers with similar thicknesses [**I**].

In the second study [**II**], all the structures composed of ZrO_2 and Al_2O_3 or ZrO_2 and $Zr_xAl_yO_z$ were deposited at 300 °C on the top of crystalline TiN bottom electrodes. $ZrCl_4$ and $Al(CH_3)_3$ were used as the metal precursors for depositing ZrO_2 and Al_2O_3, respectively, while H_2O vapor was the oxygen precursor in both cases. An additional sample set of ZrO_2-$Zr_xAl_yO_z$ structures with the $Zr_xAl_yO_z$ layer deposited using the $ZrCl_4$-$Al(CH_3)_3$-H_2O precursor pulse sequence in an ALD cycle. On the $Zr_xAl_yO_z$ layer, ZrO_2 was deposited with 80 ALD cycles employing the conventional $ZrCl_4$-H_2O precursor pulse sequence [**II**].

In the last study [**III**], HfO_2/graphene/SiO_2 and SiO_2/graphene/SiO_2 structures were engineered on the top of a TiN bottom electrodes deposited onto conductive Si substrates. First, the SiO_2 layer was deposited at 240 °C by ALD, using hexakis(ethylamino)disilane ($Si_2(HNC_2H_5)_6$) and ozone as the precursors. The graphene was grown in a home-made hot-wall CVD reactor on a copper foil that acted as a catalyst. Before starting the deposition of graphene, the reactor was heated up to 1000 °C and the copper foil was first annealed in argon and hydrogen flow for one hour to clean and recrystallize the copper surface. On this surface, graphene was formed due to the decomposition of methane when the surface exposed to the argon and methane mixture (10:1) for two hours. To transfer graphene from the copper foil to the RS structures, a polymethyl methacrylate (PMMA) support layer was first deposited by spin coating on graphene. Secondly, plasma treatment was used to remove graphene from the back side of the copper foil. As the third step, the copper foil was removed by wet etching and the resulting PMMA/graphene film was wet-transferred on the top of SiO_2 layer, dried in the air, and heat treated to soften PMMA and, hence, enhance the graphene adhesion to samples [**III**]. As the last step of the transfer, the PMMA layer was removed by dissolving it in dichloromethane [181,182]. After the graphene transfer was completed, the HfO_2 layer was deposited at a substrate temperature of 240 °C on the top of graphene. The deposition of HfO_2 was started with pretreatment using 120 H_2O pulses altered with N_2 purging pulses and followed by 120 pulses of hafnium tetrakisethylmethylamide ($Hf[N(C_2H_5)(CH_3)]_4$, TEMAHf) altered with the N_2 purges. The series of TEMAHf pulses were again followed by 120 H_2O pulses altered with N_2. After that, the main part of the HfO_2 layer was deposited by conventional plasma-enhanced ALD from TEMAHf and O_2 plasma. The pre-treatment process was important to form a buffer layer, which protected graphene from plausible damage that can be caused by O_2 plasma. It is generally known that ALD of thin films directly on the top of graphene is complicated

because, on one hand, the surface density of active adsorption sites is usually low on high-quality graphene and, on the other hand, the ALD precursors, especially ozone and oxygen plasma may destroy graphene. However, the Raman spectroscopy studies confirmed that the graphene of these structures remained intact. Additionally, the dependence of RS performance on the annealing of the bottom SiO_2 at 1000 °C before deposition of the following layers was studied. In this connection, two SiO_2-HfO_2 structures with pristine and annealed SiO_2 layers, but without intermediate graphene layers, were also prepared. In another additional sample, the HfO_2 layer was replaced with SiO_2 layer, grown by electron beam evaporation (EBE) using a SiO_2 pellet as a source material, background pressure of 2×10^{-6} mbar in the EBE chamber, and deposition rate of 0.2 nm/s. The top electrodes of Ti were also deposited by EBE while the shape of the electrodes was defined by optical maskless lithography [**III**].

The top electrodes of Pt, Ti, and Au/Ti were deposited on all RS structures using the VS-17 (Vacuumservice OY) EBE equipment. The sizes of top electrodes were defined by a physical shadow mask [**I**] or optical maskless photolithography [**II**–**III**]. Circular top electrodes with diameters of 50 μm, 250 μm and 500 μm formed an electrode matrix on a sample (Figure 4) while each top electrode defined a separate device.

For photolithography processing, the samples were spin-coated (4000 rpm, 60 s) with about 2 μm thick positive photoresist (AR-P 3510T, Allresist GmbH). The resist layer was heated on a hot plate at 100 °C for 60s and then exposed to 390 nm light using μMLA maskless photolithography equipment (Heidelberg Instruments) that defined the electrode sizes with a resolution of 0.6 μm. The lithography process was conducted in an ISO 5 cleanroom.

3.2 Composition and structure analyses

The elemental composition of the RS media was analyzed with a Rigaku ZSX 400 XRF spectrometer [**I**–**III**]. In addition, XPS studies were conducted employing a Gammadata/Scienta SES100 hemispherical photoelectron energy analyzer (in constant transmission mode) and a Thermo VG Scientific XR3E2 non-monochromatic dual Al/Mg anode X-ray gun using a Mg-K_α (hv = 1253.6 eV) X-ray excitation source [**II**], and SPECSGROUP Phoibos150 hemispherical analyzer and a Prevac RS40B1 non-monochromatic dual anode X-ray source (Al-K/Mg-K) [**III**]. The overall spectral resolution of the XPS measurements was approximately 0.8 eV.

The grazing incidence X-ray diffraction (GIXRD) method was used to characterize the crystal structure of the RS media with a SmartLab (Rigaku) X-ray diffractometer and the CuK_α radiation with a wavelength of 0.15406 nm.

The surface morphology of RS structures was studied with a high-resolution Dual Beam scanning electron microscope Helios NanoLab 600 (FEI). The focused ion beam of Helios NanoLab 600 was used to prepare lamellae for cross-section studies of RS structures with a Titan Themis 200 (FEI) transmission electron microscope.

3.3 Electrical measurements

The development of methodology for electrical measurements allowing thorough characterization of RS samples and application of the methodology for collecting information about RS in novel materials was the most important part of this thesis work. The following section gives an overview of the measurement equipment and explains how the measurements were conducted.

Although the RS phenomenon had become very prominent in development of the next-generation memory devices when this thesis work was initiated, there was still scarce information available publicly of detailed instructions on how to conduct RS measurements in practice without having earlier experience. Hence, the measurement methodology used in different studies described in this thesis was also varied to some extent while the understanding of the most efficient measurement procedure was developed gradually in the progress of the work. Correspondingly, this part of the thesis represents a considerable contribution for the unified methodology of RS studies. Some paragraphs of this section are written as general guidelines of RS measurements for researchers, who start investigation of RS properties. The information related to the repetitions and measurement parameters can be used as a recommendation for the possible choice of experimental set-up and may be adjusted depending on the purposes of the research.

3.3.1 Experimental set-up of electrical measurements

The electrical measurements of RS phenomena were carried out using a probe station MPS150 (Cascade Microtech) connected with a source-and-measure unit (SMU) 2636A (Keithley) and LCR meter E4980 (Agilent), both controlled by LabView software developed by the author of this thesis. In these experiments, tungsten probes of the probe station and triaxial cables were used to connect the top and bottom electrodes of the device with SMU (Figure 5).

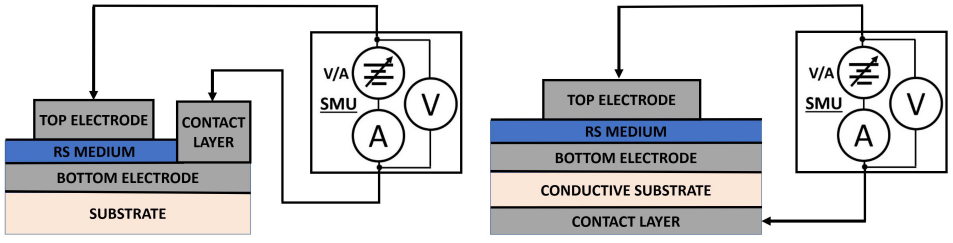

Figure 5. Schematic description of electrical measurements demonstrating probe connections from the top of the sample (left panel) and from the top and bottom of the sample (right panel) with source-measure unit (SMU).

The probe station was mounted on an antivibration table inside a shielding box specifically designed for low-current and low-voltage measurements. The shielding of the devices under measurements from electro-magnetic interference became especially important when the samples were light sensitive or measured in the

pico-ampere and sub-picoampere ranges. The probe station was also equipped with a hot plate to conduct measurements at temperatures elevated up to 300 °C.

The software enabled control of the measurement sequence, remote modification of the equipment parameters, supply of defined voltage or current to the device under tests, visualization of the data in real time, and saving the data for the later analysis. As the measurement of I-V-curves was the central tool for monitoring the electroforming process, evaluating the RS performance and determining the main parameters of RS structures (U_{SET}, U_{RESET}, I_{LRS}, I_{HRS}, and the character of the SET and RESET processes), the main focus of the software development was on the establishment of convenient measurement of I-V characteristics. Therefore, first, the software developed enabled control of voltage (or current) values and sweeping the voltage (or current) in a specified range with a specified increment/decrement value. Voltage sourcing of samples started from 0 V with a possibility to sweep up/down to ±100 V in the DC mode. However, voltages ranging between 0 to ±15 volts were generally sufficient for initial measurements of I-V characteristics.

The sweep-measurement regimes of the SMU presumed specifying several parameters. First, it had to be specified whether a sweeping list generated by the SMU following a linear or logarithmic mathematical function, or a sweeping list generated by a user was used. For the measurements using the linear or logarithmic sweeping list generated by SMU, the starting point, endpoint, voltage/current step and measurement step duration, had to be specified. These values were sent to SMU through a communication interface. According to these instructions the SMU started the required measurements and sent back the results when the sweep measurement was completed.

However, during the RS studies, real-time monitoring the I-V-characteristics is often highly desirable because the RS samples may behave unpredictably, especially during electroforming processes. Thus, the traditional sweep regime is not the best-suited one for the RS studies of unknown samples. For this reason, supplementary computer-controlled sweep functionality was implemented in the control software. This sweep functionality was based on a single-measurement command, where each measurement step was automatically sent by the control software. Two major benefits of this method were that (i) the results could be plotted as a real-time graph and (ii) the sweep could be stopped and modified at any time. Furthermore, in the single-measurement regime, the 2636A source-meter can be adjusted to supply the source voltage (or current) for the minimum time required by the instrument to measure the result. It is appropriate to mention in this connection that when measuring currents below 10 nA, the instrumental current-measurement time could extend up to 1s. Meanwhile, measurement time of currents above 1 μA can be as short as 10 μs. In the single measurement mode, these differences can be accounted and the minimum current-voltage stress to the material can be minimized.

3.3.2 Electroforming of RS devices and measurement of I-V characteristics

In order to initiate RS, the initial electroforming procedure had to be performed in most cases. To control the electroforming in real time, I-V curves were recorded during this procedure. An important step in the electroforming procedure was the determination of the voltage polarity, leading to preferential CF formation. When unknown samples were measured, the simplest way to start was to conduct symmetrical voltage sweeps at both voltage polarities. To assess the initial dielectric leakage and RS properties of the samples, approximately 10 devices, evenly distributed all over a sample, were selected. For each of these devices, the initial I-V curves were measured at rather low voltages, ranging for example from –0.8 to 0.8 V, with a voltage step of 0.01 V. The small voltage steps were chosen for precise recording the initial I-V curves. This information was useful to assess the scattering of electrical characteristics and select the devices for further studies. If non-monotonic behavior of I-V curves was observed at one of the polarities during the initial measurements, this was considered as a hint about the polarity, in which the preferential formation of CF could be expected.

CF were formed in the voltage sourcing mode. The voltage was swept in the selected direction of polarity gradually increasing the sweep amplitude. The current limit (current compliance) was adjusted to a slightly higher value than the one that the current was expected to reach at the turnback voltage, provided that no breakdown occurs. If an abrupt current change was observed or the current reached the compliance level during a voltage sweep, the forming process might have taken place. Therefore, the sweep was stopped, the sweep direction was changed, and the I-V curve was recorded again. If the I-V curve was shifted to higher absolute values of current compared with those of the initial I-V curve, a soft or hard breakdown was evident. If the change was marginal, the sweep was repeated in the initial direction with a somewhat higher current compliance value. The current compliance level was increased, and the sweeps were repeated until a significant change in resistance (at least half order of magnitude) was observed.

To find out, if the change in resistance was caused by a CF formation or hard breakdown, RESET process was attempted. At this moment it was not known whether the sample was able to attain URS, BRS or no RS. Therefore, URS was checked first. The polarity of the following sweep was kept the same that was used to cause the breakdown during the electroforming procedure. The current was not limited in the chosen voltage sweep range. If no abrupt decrease in the current took place during the voltage sweep, the sweeping range was gradually increased close to that used for electroforming. If the current decreased abruptly during the sweep, the unipolar RESET process took place. In this case, the SET process was attempted, setting the current limit at the same level that was used for forming.

If the SET process recurred, the SET and RESET switching cycles were repeated until stable switching characteristics were established by adjusting the voltage and the current compliance levels. Up to 100 switching I-V-loops were

usually recorded before the endurance and retention tests were started. It is noteworthy that the absolute values of voltages needed for RESET and SET were usually much lower than those needed for forming. For example, if the CF was formed at 8 V, the RESET and SET could have taken place at voltages around 1V and ≤ 5 V, respectively.

Sometimes, another forming/breakdown took place when the first RESET was attempted. Although it was often possible to obtain RS after several breakdowns, the resistances of LRS and HRS states, which were finally stabilized, were lower and, thus, the corresponding absolute values of currents were higher than those of the device that switched from LRS to HRS after the first forming/breakdown. Therefore, a device that suffered another breakdown instead of expected RESET was usually abandoned and the next device was selected for the further studies. In these studies, the electroforming was performed with the parameters similar to those determined from the I-V curves of the previous device. However, the maximum voltage value was sometimes adjusted because the forming voltages of different devices differed in some extent. When URS was not attainable, BRS was checked.

For testing BRS, the forming process was conducted again as described above. After the forming, the BRS RESET process was attempted. This means that the voltage was swept with the opposite voltage polarity. Current compliance was adjusted in this way that it did not limit the expected current in the chosen voltage sweeping range. If the absolute value of current decreased with increasing absolute value of voltage, the sweep direction was changed, and the SET process was reattempted. In the case of gradual RESET, the optimal RESET voltage was determined by the inspection of memory window, determined form the I-V-loops. Similar to the determination of URS voltages, the BRS voltages and SET process current compliance were adjusted until it was possible to record stable I-V characteristics of RS.

If none of the described RESET processes took place, but additional breakdowns were witnessed, then the same steps were repeated even if a device had reached the resistances that were much lower than the resistance determined for the device before the first electroforming procedure. As a rule, these measurements took a lot of time and required creative approaches to test out different possibilities before judging over the RS properties of the studied sample. In principle, this process could be compared to reverse engineering of the processor instruction set.

3.3.3 Endurance and retention measurements

The RS endurance measurements were carried out using pre-programable lists of measurement parameters. U_{SET}, U_{RESET} and current compliance values that belonged to this list were earlier identified from the I-V loop measurements. The READ voltage, U_{READ}, was added, so that the voltage was applied in succession U_{SET}, U_{READ}, U_{RESET}, and U_{READ}. U_{READ} can be set at a voltage value where the largest memory window has been observed in the I-V loops. However, the

common U_{READ} values met in the literature have ranged from –0.5 to 0.5 V. Therefore, the U_{READ} was set at 0.2 V in the majority of our experiments. As the endurance measurements were conducted in the pulsed mode, the U_{SET} and U_{RESET}, determined from the I-V loop measurements were sometimes inappropriate to complete the SET or RESET processes during a single switching pulse. Hence, in these cases, the writing voltages and pulse durations had to be adjusted during the first switching cycles performed to determine the appropriate values for these measurements.

In the measurement software, there was also a parameter that determined the number of switching cycles. Therefore, the duration of an endurance measurement was limited by this parameter or by the device itself. It is important to note that the U_{SET} and U_{RESET} often needed several adjustments to achieve more stable performance. However, the final representable result was measured with constant RS parameters. Thus, at least for one of the devices from a set of similar samples, the endurance measurements were conducted with the same set-up of measurement parameters until the failure of the device.

For the measurement of the memory state retention characteristics, the device was first switched into one of the states, i.e., to HRS or LRS, and then the state current was measured at U_{READ} over extended time. Either the I-V-loop measurement regime or writing-pulse mode was used to switch the device into the desired state. Although the retention characteristic measurement was technically one of the simplest measurements, it took a while because in most cases at least 3 hours per one state were needed to see considerable changes in the state current. Moreover, the retention measurements had to be conducted for both HR and LR states. For this reason, the control software had a specific functionality, where U_{READ}, reading interval, and measurement duration were specified. In some cases, elevated temperatures were used to study the retention, mimicking more realistic conditions of electronic hardware. Using higher temperatures, for example those exceeding 80 °C, it was possible to demonstrate the robustness of RS in some materials and reduce the time needed for the retention measurements.

4. RESULTS AND DISCUSSION

The analysis and discussion presented below follow the chronological order of conducted research. In the first study [**I**], TiO_2 and Al_2O_3 multilayered structures prepared in single deposition process were chosen as rather few studies had been devoted to RS in such structures. Earlier results demonstrated that TiO_2 epitaxially grown on RuO_2 could exhibit notably high dielectric constant and low leakage current densities [105], whereas Al doping of such TiO_2 films even more significantly reduced the leakage current densities [183]. The latter aspect linked these structures to special interest of this thesis because the epitaxial growth of the RS medium on a bottom electrode and doping of TiO_2 with Al was expected to enable reduction of power needed for switching RS devices to LRS and HRS.

The second study [**II**] was inspired by mature high-k material ZrO_2-Al_2O_3-ZrO_2 structures known in the DRAM industry under the acronym ZAZ [133]. Multilayer ZrO_2:Al_2O_3 structures were chosen at the first place as rather few works have been devoted to RS of such structures [**II**]. By incorporating deposition technology and experience from the first study [**I**], a novel approach for ALD of Al-doped ZrO_2 was applied and RS performance of dielectrics containing layers of this kind of material was studied.

The third study [**III**] is focused on application and compatibility of a two-dimensional material, graphene, in a RS structure in conjunction with the ALD-grown thin solid films. Motivated by a study of Zhang *et al.* [184], where RS structures based on graphene oxide and SiO_2 demonstrated superior endurance, and existing know-how on deposition of HfO_2 on graphene [181], RS structures based on various combinations of SiO_2, graphene, and HfO_2 were fabricated and characterized. Although fabrication of structures incorporating graphene between oxide layers is generally a challenging task, previous studies demonstrated that graphene can be used to modify the RS performance [181,182]. Thus, such structures became of high interest in relation to this thesis work.

4.1 TiO_2-$Ti_xAl_{1-x}O_y$/RuO_2 based resistive-switching media

4.1.1 Structure and composition of TiO_2-$Ti_xAl_{1-x}O_y$/RuO_2 based resistive-switching media

Al doping of rutile-phase TiO_2 has been proven to reduce leakage currents owing to compensation of oxygen vacancies and increase in effective band-gap energy of the dielectric [185]. The goal of this work was to investigate the effect of modest Al doping on the RS performance of TiO_2. Although, it has been observed that an intermediate Al_2O_3 layer may distort the crystal lattice of TiO_2 during its growth [133], it is important to mention that TiO_2 crystalized in the rutile phase [**I**], which in general is not a common phase obtained at a deposition temperature of 350 °C used in these experiments. The rutile phase was achieved due to application of rutile-phase RuO_2 as a bottom electrode that, according to

the results of earlier studies, promoted epitaxial growth of TiO_2 in the rutile phase regardless of Al doping [183]. The Al doping did not interrupt the crystal growth, evidently because $Ti_xAl_{1-x}O_y$ ($0.4 < x < 1$) instead of Al_2O_3 was used for atomic layer doping, the dopant layer thicknesses never exceeded few molecular layers of $Ti_xAl_{1-x}O_y$, and the mean Al content in dielectric was relatively low. The Al content expressed as the mean Al/(Al+Ti) atomic ratio, calculated from the results of XRF analysis, ranged from 0.03 to 0.13 in correlation with increasing number of ALD cycles applied for the deposition of $Ti_xAl_{1-x}O_y$ [**I**]. The thicknesses of resulting RS media ranged from 10 to 11 nm based on the results of the XRF analysis [**I**]. Thicknesses evaluated from the high-angle annular dark-field (HAADF) TEM images confirmed the results calculated from XRF data [**I**]. Furthermore, the energy dispersive X-ray analysis, performed in the scanning TEM mode, illustrated that to some extent, the Al had diffusively distributed from $Ti_xAl_{1-x}O_y$ layer into neighboring TiO_2 layers [**I**]. This reduced the local concentration of Al and, thus, the possible constraints to the epitaxial growth of rutile phase in the films.

The TiO_2-$Ti_xAl_{1-x}O_y$/RuO_2 structures also served as a good material to get understanding about the complexity of RS behavior, as RS was relatively easily obtained in these structures. However, attaining sufficient stability of switching was not a simple task. In the next section, examples are given to demonstrate some specific features of RS processes and propose some possible explanations for this kind of performance of RS media. Further sections will mainly focus on the RS performance of the media and discuss the plausible mechanisms in more detail than in a publication [**I**] that this part of the thesis is based on. The data of electrical measurements is the main source of information to describe and discuss the mechanisms that may have been responsible for the RS in these structures.

4.1.2 Electrical characteristics of memory cells with TiO_2-$Ti_xAl_{1-x}O_y$-based resistive-switching media

The studied samples demonstrated BRS at voltages below ±2 V and current remaining below 1 mA. The initial RS I-V curves demonstrated that such structures could perform RS even at current levels below 20 μA. However, at such low power operation the RS was not very stable. This result coincided with the trend, demonstrated by Chen [16], that scaling down the operation current of filamentary based RS devices severely degrades the RS stability, retention, and endurance. Nevertheless, the achieving RS at such low currents is a highly promising result and the further optimization of these structures should be investigated. Furthermore, an earlier study by Banerjee *et al.* [68] demonstrated that in TiO_x/Al_2O_3 bilayer structures, thinner Al_2O_3 layer enabled reduction of the RS voltages at the expense of lower HRS/LRS ratio. In the present study, RS structures with thin $Ti_xAl_{1-x}O_y$ layers embedded in between thicker TiO_2 layers demonstrated even lower RS voltages plausibly owing to a lower Al concentration which is in agreement with Banerjee *et al.* [68]. The present study also

demonstrated that increasing the number of spatially dispersed $Ti_xAl_{1-x}O_y$ layers in TiO_2 structure caused a decrease in the HRS currents. For example, the HRS current measured at 0.2 V decreased from 100 nA to 10 nA, approximately, with increasing the number of $Ti_xAl_{1-x}O_y$ layers from three to four [**I**]. Furthermore, the additional $Ti_xAl_{1-x}O_y$ layer also improved the HRS/LRS ratio, increasing the ratio from 100 to 250 approximately [**I**]. On the other hand, the samples with one but somewhat thicker $Ti_xAl_{1-x}O_y$ layer in the middle of the RS medium tended to demonstrate more stable RS repeatability and higher endurance than the samples with distributed $Ti_xAl_{1-x}O_y$ layers did [**I**]. For example, the RS structure where 4 ALD cycles of $Ti_xAl_{1-x}O_y$ were evenly distributed between the TiO_2 ALD cycles, demonstrated noticeable decay of memory window within 2500 RS cycles [**I**]. In contrast, the sample with one layer deposited by 4 consecutive ALD cycles of $Ti_xAl_{1-x}O_y$ retained its memory window after 4000 RS cycles [**I**]. At the same time, the difference in the spatial distribution of $Ti_xAl_{1-x}O_y$ in the RS medium did not seem to affect the retention of RS states.

Most of the studied samples did exhibit CW and CCW BRS. Although the top and bottom electrodes were different, the RS media had rather symmetrical structures, which could explain this behavior. Another reason for this kind of performance is the insufficient difference in the work functions of electrodes that are around 5.6–6.4 eV for Pt [186] and ~5 eV for RuO_2 [187]. The existence of possibilities for CW as well as CCW BRS might have been one of the causes of instabilities of RS behavior witnessed. However, some of the samples exhibited more stable RS in one of the directions (CW or CCW) [**I**]. Herein, it should be mentioned, that this direction preference can be affected by the initial voltage probing (initial forming) used. However, even if the device was formed and switched in opposite direction, the device eventually changed the RS direction. Because the performance of the latter devices degraded, ending up at unstable switching or narrow memory window, no further attention was focused on these devices.

To illustrate the instabilities, Figure 6 depicts three different gradual processes for a sample with a dielectric where the $Ti_xAl_{1-x}O_y$ layer was deposited using three ALD cycles. The RS I-V curve measurements started from the RESET procedure that followed the initial forming at negative voltages. The RESET of resistance took place at the positive voltage bias. Hence, CW BRS was obtained in the sample. In Figure 5, gradual shrinking of memory window can be noticed, considering that the lighter I-V curves were recorded in the beginning and the darker curves were recorded in the end of cyclic sweep measurements. In addition, gradual RESET process came up. When the voltage was increased from 0.6 V to 1 V, the current gradually decreased. Further increase of voltage caused an increase in the current. However, the resistance still increased. The latter effect indicates that the RESET process was not completed at 1V and an excess voltage (of around 0.3 V) had to be applied to achieve more stable RS.

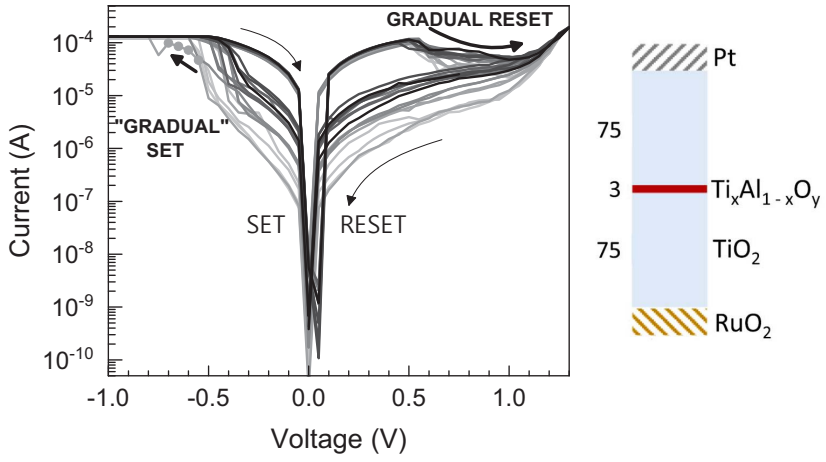

Figure 6. I-V characteristics of a sample with a single $Ti_xAl_{1-x}O_y$ layer in the middle of a TiO_2-based RS medium. The $Ti_xAl_{1-x}O_y$ layer was deposited using 3 ALD cycles. The color shading from gray to black represents the measurement succession from the beginning to the end of the measurement procedure. The loops demonstrate gradual SET and RESET as well as shrinking the memory window during the measurements.

The SET that took place under the negative voltage bias was also a gradual process. However, in this case, the process seemed to be faster than the response of the current measurement unit. Assuming that the faster switching process could have caused instantaneous current limit overshoot, it could be a cause why the RESET procedure required excess voltage to be applied. It can be speculated that, there were concurrent RS regions that could act as CCW BRS channels. Applying the above-mentioned excess voltage enabled dampening these kinds of concurrent processes.

Figure 7 demonstrates a rather remarkable range of resistance states with overall difference of almost 7 orders of magnitude in the current scale. Similar characteristics are common to media that do not exhibit acceptable RS properties, with the difference that usually the resistance is initially high and sequential forming procedures, each followed by unsuccessful RESET procedure, cause similar switching to states with lower resistance, i.e., the resistance of the device decreases as a result of each SET-RESET cycle. However, here the change of resistance states took place in increasing order (sequential RESET processes) and the fifth step shown in Figure 7 demonstrated that the device was still able to perform the SET operation.

In the early stages of this work, there was an interest in the electrical capacitance measurements of RS devices in different resistance states. However, the measurements were not successful. It turned out that the capacitance measurements, which were performed at a frequency of 10 kHz did RESET the device to the high resistance state, even if the AC signal voltage as low as 10 mV was used in these measurements. After the RESET, the current values were similar to the ones represented by the red curve in ±1 V range of Figure 7. Therefore, it seems that the AC measurement caused complete dissolving of the CF. After that it was

not possible to continue RS with previous sweep conditions as the device needed electroforming and initiating RS from the beginning. For this reason, it was not possible to evaluate plausible difference in capacitance of RS states. However, the effect could be applied to interrupt leakage channels in dielectrics or to reset RS device to the pristine-like state. Therefore, the effect of the AC signal amplitude on this kind of RESET process was characterized in more detail (Figure 8).

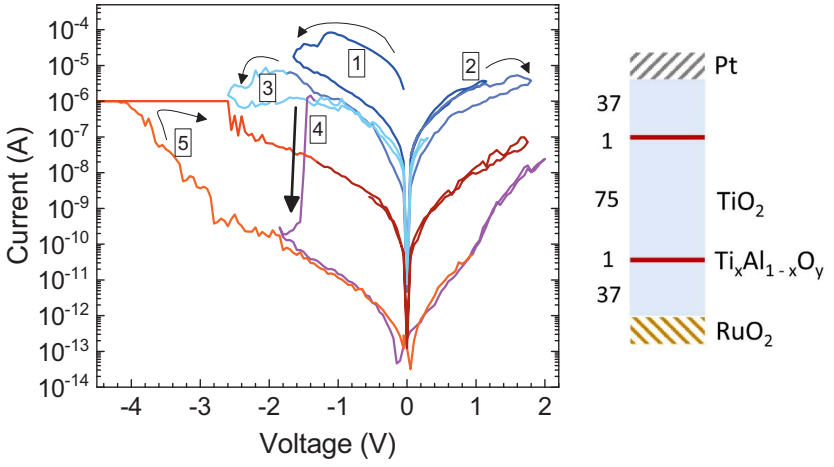

Figure 7. Unconventional RS performance of a sample, where the $Ti_xAl_{1-x}O_y$ layers were symmetrically spaced in the TiO_2-based dielectric as shown in the right panel. In steps 1–4, RESET process takes place, regardless of the voltage polarity. At step 5 the sample performs SET procedure.

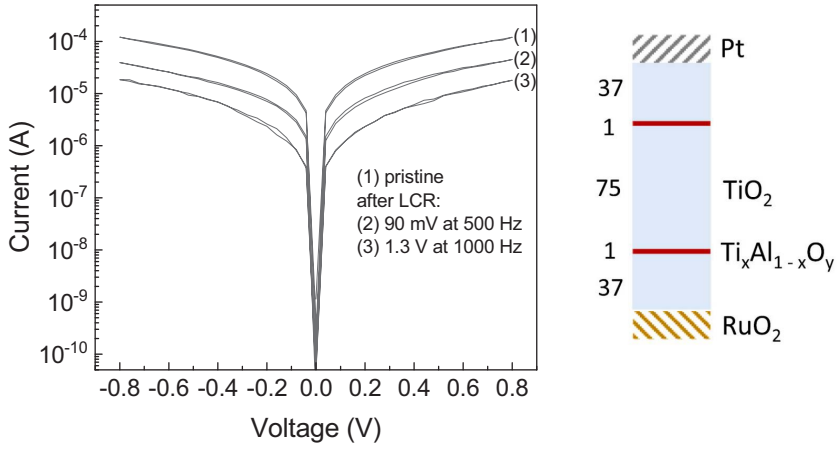

Figure 8. Influence of AC biasing on I-V curves of a RS device switched into LRS. (1) I-V curve in LRS recorded before AC biasing, (2) I-V curve after conducting capacitance measurement with 0.09 V AC signal at 0.5 kHz, and (3) I-V curve after capacitance measurement with 1.3 V AC signal at 1 kHz.

For these studies, one of the measured devices was switched into LRS and AC voltages with different amplitudes were applied for few minutes. The I-V curves were intentionally measured at low voltages to find out if the RESET procedure was effective. As can be seen in Figure 8, significant reduction of current was obtained due to AC treatment. It is possible that the RESET procedure was caused due to some unipolar RS mechanisms although these samples did not attain clear and repeatable URS during the recording of I-V curves in the usual voltage sweep mode. This conclusion is supported by the results of Kim *et al.* [62] demonstrating improvement of URS endurance by conducting URS at positive and negative polarities in a specific sequence to balance the oxygen ion drift in (and around) the RS filaments. The RS medium in the study of Kim *et al.* [62] was anatase-phase TiO_2, whereas the CFs were identified as Magneli phases Ti_4O_7 and Ti_5O_9 by high resolution transmission electron microscopy. In our study, however, the TiO_2 was grown in rutile phase and as revealed the data of Murakami *et al.* [188], who studied the nanoscale conductance of similarly prepared TiO_2 rutile films, the grains rather than the grain boundaries were more conductive. Although the CF composition and phase of our samples are not known, it may be assumed that the conductive grains form intrinsic CF and the RS itself may take place at the interface between the grain and an electrode. Independently of whether the CF formed completely through the defective grain boundaries or through connections with conductive grains, the oxygen ionic drift and oxygen vacancy formation evidently plays an important role in the switching. For example Park *et al.* [189] have demonstrated that the post-deposition heat treatment causes oxygen-related change in stoichiometry of ruthenium oxide and affects its effective work function. It is possible that the concentrated Joule heating has a similar effect. Although the Pt top electrode itself is chemically inert, the preferred CW RS of the present samples coincides with deduction by Kleiman *et al.* [150] that RESET at positive voltage bias is indicative that Pt-TiO_2 interface is the active interface. At the same time the RuO_2 bottom electrode may also contribute to RS as chemically active electrode, especially due to its ability to chemisorb oxygen as demonstrated Kim *et al.* [190]. The results of Kim *et al.* [190] also demonstrate that oxygen-saturated ruthenium oxide surface may have work function as high as 7.4 eV, which is even higher than the Pt work function. Although no clear connections can be made based on the existing data of this study, it can be hypothesized that this kind of changes in the ruthenium oxide work function may explain why the TiO_2-RuO_2 interface can became the active one and cause unexpected changes in the RS direction.

4.1.3 Conclusions on performance of TiO_2-$Ti_xAl_{1-x}O_y$-based resistive switching media

The novel atomic-layer doping process enabled revealing the effect of low concentration (< 0.14%) and small variation of Al doping on RS properties of thin TiO_2 films with the rutile phase that has not been studied earlier. It can be concluded that slight increase in Al concentration dispersed in the TiO_2 host

medium increases resistance in HRS enabling widening of the memory window (I_{LRS}/I_{HRS}). However, the samples with spatially concentrated Al doping exhibited better RS endurance. In general, these samples did not attain very stable RS performance, probably because of possibility to activate CW as well as CCW BRS mode and concurrence of these RS modes. As the number of studies related to RS of structures with RuO_2 electrodes and related epitaxially promoted growth of TiO_2 in rutile phase is scarce, the possible influence of these electrodes on RS and further optimization of such structures should be investigated more thoroughly in the future.

4.2 ZrO_2:Al_2O_3 and $Zr_xAl_yO_z$-ZrO_2-based resistive-switching media

4.2.1 Structure and composition of ZrO_2:Al_2O_3- and $Zr_xAl_yO_z$-ZrO_2-based resistive-switching media

It has been shown that layered stacks of ZrO_2 and Al_2O_3 films can successfully be grown on 3D electrode substrates, providing DRAM cell matrices with elevated bit densities [138]. Therefore, within the scope of this study, experiments were aimed at testing multilayer structures containing ZrO_2 and Al_2O_3 as components of solid media potentially functional in cells for RS devices [**II**]. During this study a sample set was prepared to study how application of $Zr_xAl_yO_z$ buffer layers could change the performance RS structures compared to that of dielectrics deposited using 6 and 30 ALD supercycles with ZrO_2 to Al_2O_3 cycle ratios of 24:1 and 4:1, respectively. Application of $Zr_xAl_yO_z$ layer was inspired from the results obtained in the previous study where the novel doping process, allowing more uniform distribution Al in the films, was used [**I**]. However, in this case [**II**], the studies were focused on asymmetric configurations because of the assumption that the symmetric structures might be less stable due to concurrent contribution of CW and CCW bipolar RS [**I**].

The thicknesses of RS media for all the studied samples [**II**] were in the range of 12–15 nm. The XRD measurements of ZrO_2:Al_2O_3 structure with ALD cycle sequence ratio 24:1 resulted in formation of metastable cubic and/or tetragonal polymorphs which are the most appropriate phases of ZrO_2 used as a dielectric in DRAMs or field-effect transistors [**II**]. The same phases were formed in the $Zr_xAl_yO_z$-ZrO_2 samples with the $Zr_xAl_yO_z$ buffer layers. However, the latter samples exhibited higher crystallinity compared to that of the former one. The higher crystallinity can be attributed to the growth of less distorted lattice in the top ZrO_2 layer of the $Zr_xAl_yO_z$-ZrO_2 structures compared to the lattice in the alternately layered ZrO_2:Al_2O_3 films.

The XRF measurements [**II**] indicated higher aluminum content in the films composed of alternating ZrO_2 and Al_2O_3 layers, which can be expected based on the ALD cycle sequence. On the other hand the residual Cl content originating from the Cl-based Zr precursor was higher in the $Zr_xAl_yO_z$-ZrO_2 films, which can

be accounted to successive exposures of the surface to $ZrCl_4$ and $Al(CH_3)_3$ without intermittent supply of oxygen precursor [**II**]. However, the content of chlorine present in the films was low and, for this reason, had no measurable effect on RS performance. The XPS analysis from the measurements of a reference sample with the RS medium that contained only the $Zr_xAl_yO_z$ layer further indicated likely presence of oxygen vacancies [**II**].

4.2.2 Electrical characteristics of memory cells with ZrO_2:Al_2O_3- and $Zr_xAl_yO_z$-ZrO_2-based resistive-switching media

Well-defined RS cycles with I_{LRS}/I_{HRS} ratios close to 10^5 in the electrical current scale were recorded for the sample with the alternating ZrO_2:Al_2O_3 RS medium, deposited with cycle ratio of 24:1 [**II**]. This sample also demonstrated the highest relative permittivity (k > 35) amongst the studied samples [**II**]. Despite the promising I_{LRS}/I_{HRS} ratios, the sample exhibited poor RS endurance of less than 25 RS cycles [**II**]. The sample attained RS in the CW direction, i.e., the switching to LRS took place at negative voltage polarity. The currents in LRS exceeded 1 mA at U_{RESET} (2–2.8 V) which may have caused too high I-V stress leading to hard breakdown [**II**]. At the same time, there was a device on the same sample that showed unexpected CCW RS (Figure 9) at a voltage of around –0.8 V as a partial RESET during a sweep leading to the SET operation.

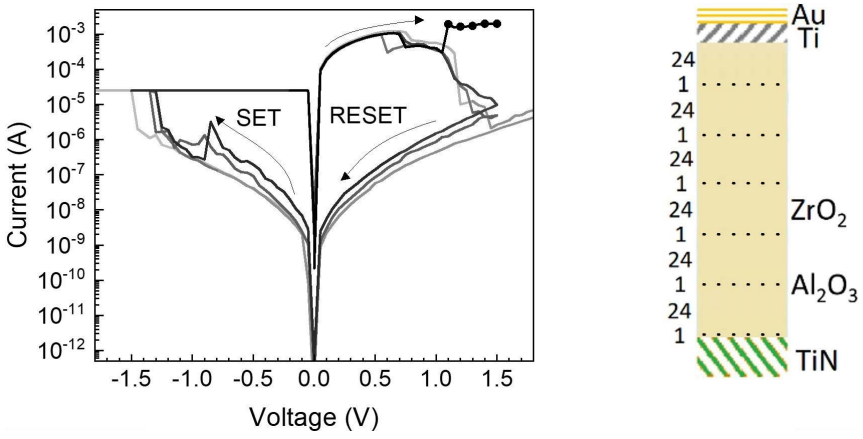

Figure 9. RS I-V curves of a sample with ZrO_2:Al_2O_3 RS medium deposited repeating supercycles that contained 1 and 24 ALD cycles for synthesis of Al_2O_3 and ZrO_2, respectively. To extend the number of switching cycles the SET current limit was set at 25 μA. The dotted part of the curve indicates dielectric hard breakdown during the RESET procedure. The color shading from gray to black represents the measurement succession from the beginning to the end.

Figure 9 also visualizes an unsuccessful attempt to reduce the I-V stress by limiting the SET-process currents more vigorously. Comparing Figure 9 with Figure 9 (a) in the earlier publication [**II**], one can see that the reduction of the SET current

limit did decrease the RESET currents nearly by one order of magnitude whereas U_{RESET} decreased from ~3 V to 1.5 V. The RESET process visualized in this work (Figure 9) took place gradually compared to abrupt RESET of the same structure shown in the publication [**II**]. Unfortunately, these improvements had even a detrimental effect on the endurance as only 4 successful switching cycles could be completed (Figure 9). This performance can be explained by reformation of weaker filaments due to vigorous limiting of SET currents [16]. It is appropriate to remind that the RESET current cannot be confined in such manner as this kind of current limitation hinders the RESET procedure or makes it unreliable. It is also worth noting that the sample represented in Figure 9 demonstrated gradual RESET which referred to the possibility of achieving multilevel RS. There was also a sample with the RS medium, deposited using the ZrO_2:Al_2O_3 ALD cycle ratio 4:1, that yielded multilevel RS with 3 distinguishable resistance states [**II**]. Unfortunately, the latter sample also suffered from poor endurance [**II**].

The $Zr_xAl_yO_z$-ZrO_2 structures with $Zr_xAl_yO_z$ buffer layers demonstrated relative permittivity between 25 to 35 [**II**]. This sample set demonstrated endurance of more than 5000 RS cycles [**II**]. Here it should be mentioned that these samples were prepared after initial electrical measurements of ZrO_2:Al_2O_3 structures indicating poor RS endurance. Therefore, it was also hoped that inserting a thin layer with higher concentration of Al into the structure could improve the RS endurance similarly to the previous study [**I**]. Although the memory window of the latter samples was approximately one order of magnitude in the current scale, these samples could be considered to have better RS performance than the ZrO_2:Al_2O_3 samples [**II**]. The $Zr_xAl_yO_z$-ZrO_2 sample, in which the $Zr_xAl_yO_z$ buffer layer was deposited with one ALD cycle, also exhibited CW BRS, i.e., switching to LRS took place at a negative bias (Figure 10, left panel). In contrast, the samples with the buffer layers deposited using more than one ALD cycle exhibited CCW BRS (Figure 10, right panel) [**II**].

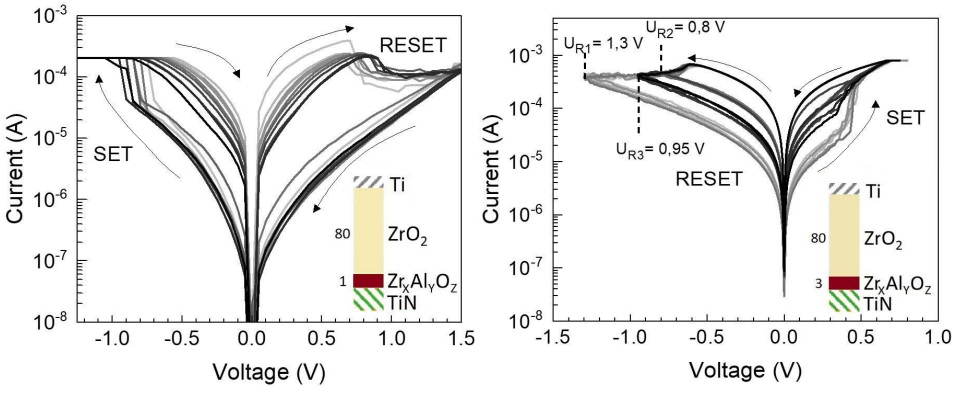

Figure 10. RS I-V characteristics of Ti/ZrO_2/$Zr_xAl_yO_z$/TiN structure, where $Zr_xAl_yO_z$ buffer layer was deposited by applying one (left panel) and three (right panel) ALD cycles, demonstrating CW and multilevel CCW BRS operation, respectively. Transition from grey to black on the left panel indicates succession of I-V measurement cycles.

It should be mentioned in this connection that one ALD cycle yielded less than one monolayer of $Zr_xAl_yO_z$. The nonuniformity of this layer may be one of the reasons why the sample demonstrated CW-RS. Considering that the sample with the ZrO_2:Al_2O_3 insulator also exhibited CW-BRS, some hypothetical aspects can be discussed. For example, if one considers the oxygen vacancies or oxygen diffusion and electric-field induced drift as the main cause of RS, some plausible dynamics can be discussed [191]. In the electric field, the oxygen ions with negative charge are attracted towards the positive potential. In the case of CW-RS, the SET operation is obtained at a negative bias applied to the top electrode. This means that CF is formed because of oxygen attraction towards the bottom (TiN) electrode and formation of oxygen-deficient channel in the dielectric. The SET process is completed when the oxygen-deficient filament extends up to the top electrode. During RESET, taking place at a positive bias applied to the top electrode with respect to bottom electrode, the oxygen ions diffuse/drift back towards the top electrode and recombine with the oxygen vacancies created in CF during the SET process. The most significant changes in the CF resistance plausibly occur near the interface between the dielectric and the top (Ti) electrode. The CW-RS can be obtained, when the bottom electrode or the interface region between the RS medium and bottom electrode can getter and release the oxygen ions dependently on the direction of the electric field applied. There are evidences that oxide layer may form on TiN due to exposure to air [192]. Hence, this oxide layer could be formed in the RS process, as well, while the oxide layer formed may act as an oxygen reservoir supporting CW-RS.

Considering the circumstance that the buffer layer thickness influenced the RS direction, it can be assumed that in the case of thicker buffer layers, when CCW-RS was obtained, the interface between the TiN and dielectric could not act as an efficient oxygen reservoir anymore. Instead, the gettering and release of oxygen that depended on the electric field direction was probably more efficient at the interface between the dielectric and the top (Ti) electrode. Correspondingly, the CF rupture took place at the interface between the dielectric and bottom (TiN) electrode. The oxygen gettering ability of Ti is often related to the formation and rupture of conductive filaments [110]. The conclusion that dielectric-electrode has an important role in determining the performance of a RS device is supported by the data of Wang *et al*. [193] who demonstrated that embedding additional Mo metal layer between Ti and ZrO_2 to induce more oxygen vacancies, resulted in forming-free CCW BRS.

The plausibly lower defect concentration at the Ti/ZrO_2 interface compared to that at the $Zr_xAl_yO_z$/TiN interface may explain the markedly wider memory window of the structures showing CW-RS ($I_{LRS}/I_{HRS} \approx 10^5$ and $I_{LRS}/I_{HRS} \approx 10^2$ measured at 0.2 V for RS structures represented in Figure 9 and Figure 10, left panel, respectively) compared with the memory windows of the structures with thicker $Zr_xAl_yO_z$ buffer layers ($I_{LRS}/I_{HRS} \approx 20$ measured at 0.2 V for the RS structure represented in Figure 10, right panel). In the former case, the CF rupture takes place in the region where the possible detrimental effect of the substrate surface on the growth of dielectric was small while in the latter case, the CF rupture is

obtained in the interface region that was formed in the beginning of deposition and, for this reason, was expected to be more defective.

Supplementary RS state retention measurements were carried out for two samples with $Zr_xAl_yO_z$ buffer layers deposited using 3 and 5 ALD cycles (Figure 11).

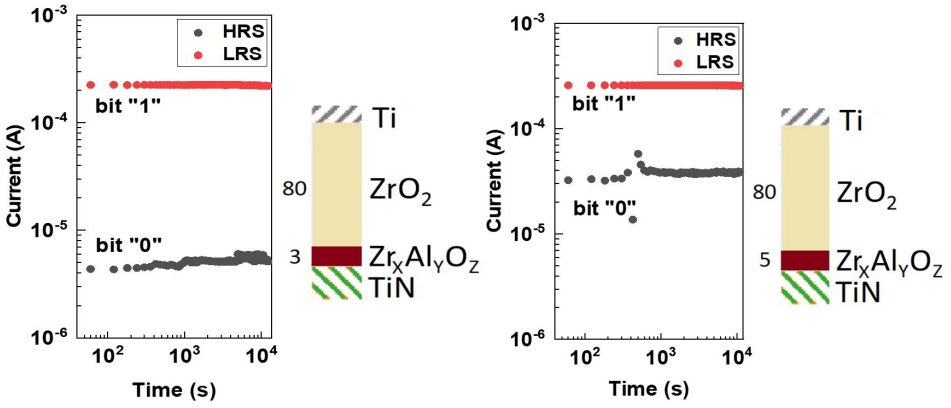

Figure 11. RS state retention characteristic measured at 80 °C and U_{READ} = 0.2 V for asymmetrical structures with $Zr_xAl_yO_z$ buffer layers deposited using 3 (left panel) and 5 (right panel) ALD cycles.

The RS I-V characteristics measured prior to retention studies confirmed the device to device repeatability reported in the earlier publication [**II**]. At 80 °C, both devices retained their HRS and LRS states during 3 hours approximately. After the retention measurements RS I-V characteristics were measured from both devices to confirm the further switching capability. For the sample with $Zr_xAl_yO_z$ buffer layers, deposited with three ALD cycles, multilevel RS performance was attained. The multilevel RS was achieved by setting the RESET voltage to the values (–0.8 V and –0.95 V) that were lower than those required for full RESET. Figure 12 demonstrates the LRS and HRS current values extracted from the I-V characteristics measured during the heating up and cooling down the latter sample, while keeping the sweep parameters unchanged.

The left panel of Figure 12 shows, how the memory window increased because of the HRS current decrease upon heating the sample from 22 °C to 80 °C. The latter may be temperature accelerated work-in process, as it is common that the initial memory window increases due to the optimization of the switching voltage and SET process current limit. During the cooling down (Figure 12, right panel) the I-V loop RESET voltage was chosen –1 V instead of initial –1.3V as a precaution after the sample had been heated in total more than 6 hours. The memory window demonstrated minor shrinking. Nevertheless, the memory window during cooling was comparable to above mentioned multilevel state of RS with RESET voltage of –0.95 V, measured already at room temperature. The higher temperature HRS currents ($<10^{-5}$) were restored after increasing the RESET voltage to initial –1.3 V that is shown on the I-V characteristic (Figure 10), which was recorded at room temperature after retention measurements.

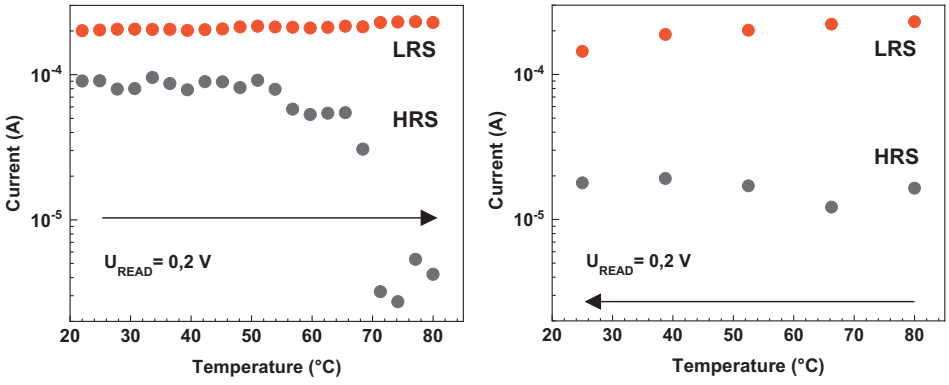

Figure 12. HRS and LRS currents extracted from I-V characteristics of during heating the sample up to 80 °C (left panel) and cooling after retention measurements to 25 °C (right panel) to demonstrate that the sample with Ti/ZrO_2/$Zr_xAl_yO_z$/TiN structure, where $Zr_xAl_yO_z$ buffer layer was deposited by applying three ALD cycles retained its memory window after cooling.

4.2.3 Conclusions on performance of ZrO_2:Al_2O_3- and $Zr_xAl_yO_z$–ZrO_2-based resistive-switching media

There are very few RS studies devoted to periodic ZrO_2:Al_2O_3 structures obtained by ALD. Majority of those are related to generally known good dielectric properties of these structures. However, the present study demonstrated that such structure could attain rather large memory window with $I_{LRS}/I_{HRS} \approx 10^5$ [**II**]. Unfortunately, the devices with these RS media had poor RS endurance (< 30 cycles) and, thus, it was proposed that asymmetric configuration where low Al concentration is attained in structurally more defective buffer $Zr_xAl_yO_z$ layer combined with a ZrO_2 layer may improve the RS parameters such as endurance. The application of a novel ALD process, similar to that exploited for deposition of $Ti_xAl_yO_z$ in the previous study [**I**], enabled tailoring a novel structure which demonstrated more stable resistive switching, multilevel performance with appreciable endurance and retention properties. Although the $Zr_xAl_yO_z$–ZrO_2 films contained similar metastable cubic and/or tetragonal phases and had only slightly lower dielectric permittivity compared to the ZrO_2:Al_2O_3 structures, the former suffered from narrower memory window. Thus, further optimization of these structures is required.

4.3 HfO_2-graphene-SiO_2-based RS media

4.3.1 Structure of HfO_2-grapene-SiO_2 based resistive-switching media

This study was focused on the application of graphene in HfO_2/graphene/SiO_2 and SiO_2/graphene/SiO_2 RS media [**III**]. In one of the earlier studies [182], we demonstrated that inserting graphene layer between the host ZrO_2 medium lowered the currents at which RS took place. Compared to the sample without graphene, the difference between LRS and HRS was slightly higher in the case of sample with graphene layer while the required switching voltages were higher (by 0.5 V approximately) [182].

In this study, five structures differing from each other in some aspect of preparation were investigated. The complete sample set is visualized in the Figure 13. The graphene layer separating two different dielectric layers was purposefully used to induce defects in the upper dielectric layer [**III**]. Moreover, the graphene layer was expected to work as an ion blocking layer affecting RS device power consumption [194].

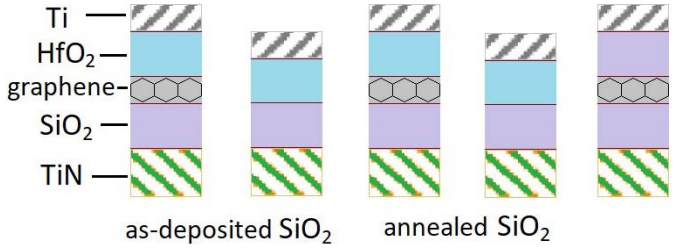

Figure 13. Schematic structure of electrically evaluated samples with HfO_2/graphene/SiO_2, HfO_2/SiO_2 and SiO_2/graphene/SiO_2 dielectrics.

The first SiO_2 layer deposition process yielded amorphous film with a density of 1.8 g/cm^3 measured for an as-deposited 8 nm thick films by the X-ray reflection analysis method [**III**]. Annealing the samples at 1000 °C in an argon environment resulted in densification of the SiO_2 layer to 2.3 g/cm^3 while the thickness decreased to 6.3 nm [**III**]. The chemical composition, studied by XPS, corresponded to the stoichiometric SiO_2 [**III**]. Raman spectroscopy studies of the samples performed after the graphene transfer revealed no detectable amounts of structural defects in the graphene layer. The SEM images of the HfO_2 layer demonstrated granular structure of the surface, indicating that the film growth on top of the graphene started at spatially separated adsorption sites. This kind of growth plausibly contributed to the formation of additional structural defects [**III**]. The quality of the graphene was assessed by the Raman spectroscopy also after the deposition of the top HfO_2 and SiO_2 layers as both HfO_2 and SiO_2 were highly transparent for the light used in the Raman spectroscopy studies. Some indications of structural defects in graphene became evident after the deposition of the HfO_2 layer but in general, the graphene remained intact [**III**]. In the samples

where the amorphous SiO_2 was deposited on top of graphene, the structural defects of graphene did not appear [**III**].

4.3.2 Electrical characteristics of memory cells with HfO2-graphene-SiO2-based resistive-switching media

The sample, where the dielectric layer between Ti top and TiN bottom electrode was composed of as-deposited SiO_2 and HfO_2 without graphene (Figure 13, second panel), demonstrated highly insulating properties. Relatively high voltages ranging from –60 V to 40 V were applied and no RS or dielectric breakdown was witnessed. The latter result could be expected as both materials SiO_2 and HfO_2 are known to have good dielectric properties. However, the similar sample, where the SiO_2 layer was annealed before the HfO_2 deposition (Figure 13, fourth panel) demonstrated modest RS properties (Figure 14).

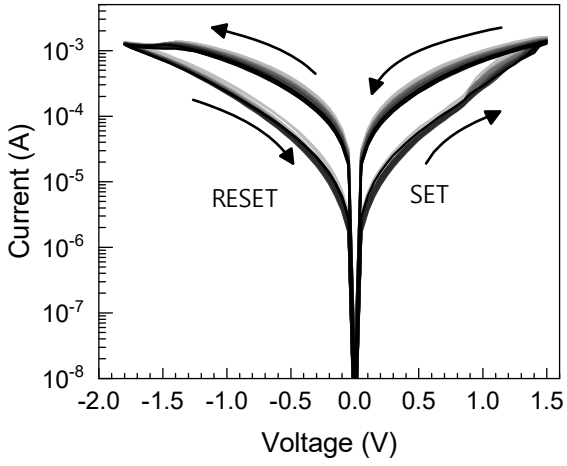

Figure 14. RS I-V characteristics of Ti/HfO_2/SiO_2/TiN structure, with the SiO_2 layer annealed at 1000 °C. Transition from grey to black indicates succession of recording the I-V cycles. During the first RS cycles the gradual SET process starting at 0.9 V showed steeper slope than that recorded during the following cycles. The maximum currents determined at 1.5 V were limited by the sample itself [**III**].

The RESET process was reproducible. However, complications of achieving the LRS can be seen from the RS I-V characteristics. In the beginning of the measurements, the SET process started at 0.9 V where the slope of I-V curve changed noticeably (Figure 14, gray I-V loops) whereas the slope of the last RS I-V loops remained almost unchanged (Figure 14, black curves) making impossible reaching the current compliance at voltages up to 1.5 V. As a result, the maximum currents recorded at 1.5 V were limited by the device itself. After increasing the SET process voltage to increase currents in LRS, the device suffered from hard breakdown. Another device from the same sample demonstrated similar gradual

shrinking of the memory window until complete collapse within less than 100 RS cycles. Therefore, the further and more detailed investigation of this sample did not seem to be relevant.

The sample a graphene layer between as-deposited SiO_2 and HfO_2 oxide layers (Figure 13, first panel), did show RS-like performance [**III**]. Voltage sweeps between –7 V and 7 V without current compliance caused resistance changes at random voltage values and polarities. The maximum current was about 2 µA and current compliance was not necessary as the device limited the LRS currents intrinsically. However, the current compliance was applied, when the forming procedure was attempted in the wider voltage ranges. The forming procedure was attempted at positive and negative voltage polarities on different devices, but only hard breakdown occurred. Hence no reproducible and uniform RS was observed.

The most interesting RS results were obtained from the HfO_2/graphene/SiO_2 samples (Figure 13, third panel) where the SiO_2 layer was annealed before the transfer of graphene on top of that. Although some devices did not need forming [**III**], there were devices on the same sample that had to be formed before RS studies. The formation of RS took place at 8 V, approximately, where an abrupt current increase from 60 µA to 500 µA limited by the current compliance was seen. Further RS was recorded with I-V sweeps in a voltage range extending from –0.9 V to 1.5 V (Figure 15). Consistently with the formation, the SET process took place at the positive polarity. The SET process was abrupt and the U_{SET} voltage varied between 0.9 V and 1.5 V. However, compared to the RESET process, the SET process was more stable. The RESET process took place at the negative voltage polarity with large fluctuation as can be seen from the RS I-V characteristic (Figure 15, left panel).

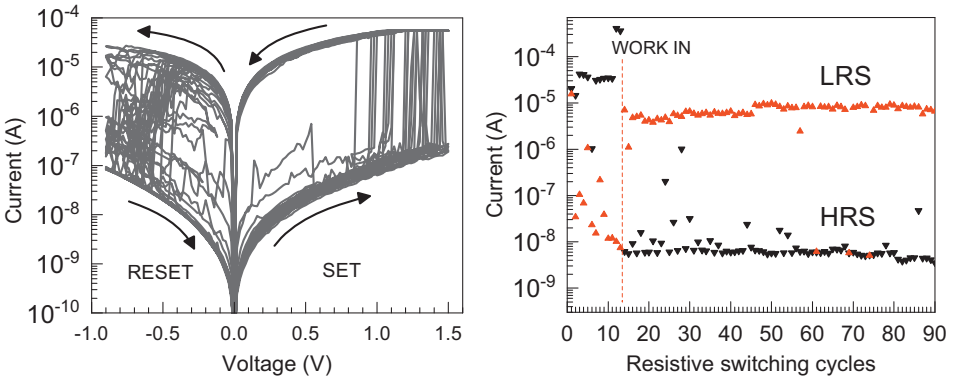

Figure 15. RS I-V characteristics (left panel) and retention characteristic (right panel) of a Ti /HfO_2/graphene/ SiO_2/ TiN structure where the SiO_2 layer was pre-annealed. [**III**]

In a recent study of Trstenjak *et al.* [195], similar structures exhibited similar CCW RS with a memory window of about 3 orders of magnitude in the current scale. In the latter study by Trstenjak *et al* [195], the graphene layer was used directly as a bottom electrode and Pt as a top electrode because the application of

Ti top electrode as an oxygen scavenger made the devices electrically too conductive and, thus, not exhibiting RS. Including the SiO_2 layer into the RS medium in our experiments enabled RS in structures with the Ti top electrode at the expense of higher HRS and LRS currents compared to those reported by Trstenjak *et al.* [195]. The amplitudes of RS voltages U_{SET} and U_{RESET} our devices were nearly half of those reported by Trstenjak *et al.* [195]. The RS endurance characteristic (Figure 15, right panel) demonstrates that the HRS and LRS currents recorded at a reading voltage of 0.2 V outline rather uniform memory window of our RS structures. Complications during RESET seem to lessen after 60 cycles, which may hint to a gradual stabilization of the RS process in these structures. The currents in HRS were about one magnitude higher ($\sim 10^{-8}$ at 0.2 V) than the corresponding current values measured before forming of the device ($\sim 10^{-9}$ at 0.2 V).

The state retention measurements, conducted at the room temperature, revealed that the LRS was volatile. The initial LRS value was retained for < 20 s. After 30 s the resistance rose to the HRS level. After approximately 1 h the device resistance raised to the initial value of the pristine sample [**III**]. These results indicate that the conductive filament degraded plausibly due to the relaxation and recombination of defects contributing to conductivity of CF. Zhao *et al*. [123] demonstrated somewhat similar nonvolatile behavior. They attributed the nonvolatile behavior to the effect of defective graphene layer in the Ag/DG/SiO2/Pt device [123]. The ECM based RS described by Zhao *et al*. [123] was non-polar meaning that the SET process took place at ±1 V and the device self-reset to HRS within 1 μs. The RS process where a resistance state changes within less than one second after removing the electric field is also known as threshold switching [169]. In the same study Zhao *et al*. [123] combined such threshold switch (Ag/DG/SiO2/Pt) in series with non-volatile BRS device as a selector device, which guarantees that the combined device as a whole is in HRS in the standby mode whereas the non-volatile device can be either in LRS or HRS. Such a combination is useful, enabling to avoid parasitic currents, i.e. crosstalk in crossbar memory matrix. However, in this study, the LRS state was retained for longer than common for threshold switches. Hence, further attention should be paid to this kind of phenomenon as it may be beneficial for application, e.g., in developing hybrid DRAM.

The additional sample, where the graphene layer was followed by SiO_2 instead of HfO_2 (Figure 13, fifth panel) demonstrated RS at unusually high voltages. The abrupt SET was observed at voltages ranging from –14 V to –30 V. However, based on the occurrence of the abrupt transition to LRS, the voltages at which the transition took place could be divided into two regions. On fewer occasions, the SET process took place at voltages ranging from –23 V to –30 V and more frequently in voltage range extending from –14 V to –23 V. The RESET process was gradual and took place rather uniformly at 9–14 V. It was not possible to identify a certain formation process as the SET process occurred several times at similar voltages, at which the device switched to the LRS first time. It is possible that the conductive filaments were destroyed almost completely by the following

RESET, when the SET process occurred at voltages ranging from –23 V to –30 V. When the switching took place at the voltages ranging from –14 V to –23 V, then the filament was only partially disrupted during the RESET process. The latter is also supported by the HRS currents, which were higher when SET occurred at voltages ranging from –14 V to –23 V.

4.3.3 Conclusions on performance of HfO_2/graphene/SiO_2-based resistive-switching media

The results of the present study demonstrate the versatility of ALD in deposition of dielectrics on graphene and indicate that application of graphene in RS structures can significantly improve the performance of those. As these samples had rather complex preparation steps, the fabrication of these structures needs further optimization to attain more uniform devices. In general, the presence of graphene in the HfO_2/graphene/SiO_2 samples had an important role in attaining RS. Although the HfO_2/SiO_2 sample with annealed SiO_2 layer enabled achieving rather stable RS, the memory window of these devices was narrow (I_{LRS}/I_{HRS} <10 at 0.2 V) and the gradual shrinking of the memory window until complete collapse resulted in poor endurance (<100 cycles). However, if the SiO_2 layer of HfO_2/graphene/SiO_2 sample was annealed before transferring graphene layer, the samples demonstrated volatile RS performance. The sample showed appreciably wide memory window ($I_{LRS}/I_{HRS} \approx 10^3$ at 0.2 V), but the LRS had poor retention (<20 s) i.e., the LRS was volatile.

5. FUTURE PROSPECTS OF RESISTIVE SWITCHING

The current interest in development of RS devices seems to be shifted towards neurocomputing, which may be the most promising application for RRAM [16,152,196]. Despite the fact that RRAM is believed to be one of the promising ones in the emerging memory technologies, there is still a long way to substitute NAND storage class memory (SLC). The writing power consumption of NAND memories (~10 fJ) is much lower, compared to the lowest power consumption (~0.1 pJ at a writing voltage of 0.5 V) reported for RRAM [2,108]. For comparison, the technological requirements specify that the power consumption of future memory technology must be <10 pJ per bit with <1V operating voltages, 10 ns writing speed and endurance $>10^9$ cycles [108,197]. Energy consumption is calculated as a product of voltage, current and time. From that, one can estimate that to achieve power consumption of 10 pJ per bit with 1 V writing voltage and 10 ns writing time the operating current should remain under 1 mA. Several comprehensive RRAM review publications demonstrate that many RS media operate at currents below 1 mA with switching voltages close to 1 V and switching times around 10 ns [16,63,108]. NOR-type FLASH consumes ~100 pJ per bit, writing at voltages >10 V with a writing speed of 10 μs – 1 ms. From that, it can be understood why RRAM can replace NOR-type FLASH. Coming back to NAND-type FLASH, the research of emerging memory technologies remains of critical importance as the aggressive scaling has led to the decrease in the number of charge trapped electrons in the floating gate, which in turn, has an detrimental effect on the reliability [6]. RRAM could be used as a substitute of NAND FLASH, if the power consumption of RRAM could further be reduced. For example, the RRAM power consumption would be <100 fJ per bit, if the switching operation takes place at currents <10 μA, voltages below <1 V, and switching pulse durations <10 ns. In one of the studies that this thesis is based on, some $Ti_xAl_{1-x}O_y$ structures demonstrated similar currents and voltages [**I**]. However, those devices also showed marked variance of the switching processes. The general problem that arises from the low-current operation is insufficient endurance and retention [16]. For instance, very short retention times were determined for HfO_2/graphene/SiO_2 RS structures that operated at relatively low currents [**III**]. Lower currents indicate formation of CF with smaller lateral sizes and/or lower concentration of electronic states contributing to the conductivity of the filament formed. For this reason, the stochasticity of RS processes is higher in this kind of structures [16,26]. Furthermore, at low currents, the random telegraph noise intrinsic to semiconductor devices becomes critical at low reading voltages increasing the current variability in the RS states [26]. Another way to reduce the energy consumption is to decrease the durations of switching pulses. Csontos *et al.* [198] recently demonstrated 20 ps writing operation of BRS based on 5 nm thick Ta_2O_3. Moreover Pi *et al*. demonstrates BRS in 6 nm thick TiO_x -HfO_2 memristor crossbar structure with single memory element electrode area of 2 nm × 2 nm which further proves the scalability of RRAM. Nevertheless, to apply RRAM in standalone SCM, RS generally requires further investigation to

understand the underlying mechanisms more quantitatively. In this connection, modelling approaches, extensively applied to widen the general understanding and to design more robust and reliable RS media [27], are also expected to support further development of reliable RRAM devices.

6. SUMMARY

In the research conducted for the present thesis, several RS structures were produced and characterized to investigate the influence of fabrication process parameters, and composition and structure of complex RS media on the RS performance of the RS MIM structures.

Characterization of RS media based on different dielectric materials demonstrated that atomic layer deposition of Al_2O_3-doped TiO_2 films on RuO_2 electrodes, promoting epitaxy of rutile-phase TiO_2, enabled fabrication of RS media with appreciably high (3 orders of magnitude) HRS to LRS resistance ratios. Both endurance and retention tests were passed preliminarily. Implications of multilevel switching were recorded. However, the stability of RS performance remained problematic.

Atomic layer deposition of wide-bandgap insulators, based on solid solutions of ZrO_2 and Al_2O_3 with periodically changing content of Al_2O_3, allowed engineering RS media possessing HRS to LRS resistance ratios up to 10^5. However, this result was evidently achieved at the expense of device endurance. In contrast, application of thin $Zr_xAl_yO_z$ interface layers on the top of TiN bottom electrodes followed by the deposition of markedly thicker Al-free ZrO_2 on these interface layers, enabled tailoring of RS structures with enhanced RS endurance. Implications of multilevel switching in these structures were recorded. Unfortunately, this improvement in endurance was accompanied by a decrease in the HRS to LRS resistance ratios.

Stacked SiO_2 and HfO_2 films grown by ALD were the widest-bandgap and structurally most stable metal oxide thin-film structures, studied in this work. The stacks were highly insulating. No possibility to reliably awake the RS effect in these structures was revealed. However, transfer of graphene sheets on an as-deposited bottom SiO_2 layer before the deposition of the top HfO_2 layer allowed one to create three-layer stacks implicating the RS effect, although stable and uniform resistive switching was not attained. Transfer of graphene on an annealed SiO_2 layer before the deposition of the top HfO_2 layer allowed one to create three-layer stacks demonstrating clear resistive switching behavior with moderate switching voltages and considerable endurance, although with poor retention characteristics.

The results of RS studies indicate that combinations of atomic layer deposited oxide films such as SiO_2, HfO_2, ZrO_2, TiO_2, Al_2O_3, and chemical vapor deposited graphene in novel multilayer or complex compounds allow one to control the RS performance of the resulting solid media. However, optimization and simultaneous improvement of the device characteristics requires careful design and tailoring of the RS media to maximize the HRS to LRS resistance ratio, reduce the switching voltages, and prolong the endurance and retention. This can be regarded as a challenge that is worth further investigations.

SUMMARY IN ESTONIAN

Takistuslülitused mitmekihilistel dielektrikutel põhinevates mälustruktuurides

Käesolevas töös uuriti takistuslülituslikku mäluefekti erinevates siirdemetallide oksiidides ja nende kihtstruktuurides. Takistuslülituslikku mälu peetakse üheks paljulubavaks tulevaseks mälutehnoloogiaks, mis võiks aidata lahendada probleeme, mis paratamatult kaasnevad mäluseadmete peamiste koostisosade, mälurakkude, mõõtmete edasise tehnoloogilise vähendamisega. Kuigi tänased mälutehnoloogiad suudavad infoajastu kiire arenguga veel mõningat aega sammu pidada, on teaduslikust perspektiivist oluline uurida uusi võimalusi, mis lubaksid parendada mälurakkude koostismaterjalide tehnoloogiliselt olulisi omadusi.

Käesoleva töö esimeses etapis, mille tulemusi on kirjeldatud esimeses artiklis [**I**], uuriti takistuslülitust titaandioksiidil põhinevates kihtstruktuurides, mis olid kasvatatud rutiili faasis ruteeniumoksiidile. Lisaks sellele, et ruteeniumoksiid on metallilise juhtivusega, olles uuritud takistuslülitusstruktuurides üks elektroodidest, soodustas rutiili faasis ruteeniumoksiid titaanoksiidi epitaksiaalset kasvu samuti rutiilina tavapärasest madalamatel temperatuuridel. Rakendades tavapärasest erinevat lähteainepulsside järgnevust aatomkihtsadestamise tsüklites, oli võimalik täiendada takistuslikult ümberlülituva keskkonna struktuuri titaan- ja alumiiniumoksiidi segu sisaldavate kihtidega, muutes sellega alumiiniumi sisaldust titaanoksiidil põhinevates takistuslülituskeskkonnas. Tänu sellise meetodi kasutamisele alumiiniumi lisamiseks oli võimalik muuta alumiiniumi kontsentratsiooni väga õhukestes kihtides suhteliselt väikese sammuga. Seetõttu oli võimalik teha kindlaks, et juba väike alumiiniumi kontsentratsiooni kasv suurendas oluliselt suure takistusega oleku takistust ning muutis seega usaldusväärsemaks suure ja väikese takistusega mäluolekute eristamise mäluelementides.

Teises etapis ja teise artikli [**II**] aluseks olevas uuringus vaadeldi takistuslülitust perioodiliselt muutuva alumiiniumoksiidi sisaldusega tsirkooniumoksiidi ja alumiiniumoksiidi segudes ja võrreldi seda takistuslülitusega dielektrikutes, mille esimeseks kihiks oli alumisele titaannitriidelektroodile sadestatud tsirkooniumi ja alumiiniumi seguoksiid ja teiseks kihiks oli alumiiniumivaba tsirkooniumoksiid. Esimesena nimetatud struktuuride mõõtmine tuvastas väga suure takistuste erinevuse suure ja väikese takistusega mäluolekute vahel. Pingel 0.2 V registreeritud voolud erinesid ligi 5 suurusjärku. Paraku oli lülituste korratavus suhteliselt halb. Seguoksiidist aluskihiga kahekihiliste struktuuride lülituste korratavus oli palju parem, kuid nendel oli takistuste erinevus suure ja väikese takistusega olekute vahel oluliselt väiksem. Need tulemused näitavad, et mitmekihiliste struktuuride kasutamise ning nende varieerimise ja optimeerimisega on võimalik oluliselt muuta takistuslülituslike keskkondade omadusi.

Käesoleva töö kolmandas etapis [**III**], mis oli ühtlasi aluseks kolmandale artiklile, vaadeldi ränioksiidi ja hafniumoksiidi sisaldavaid struktuure, mille koostisse kuulunud oksiididel puudusid lõõmutamata olekus arvestatavad takistuslülituslikud omadused. Peale lõõmutamist 1000 °C juures oli ränioksiidis võimalik

saada takistuslülitusi, kuid lülituste korratavus oli väike. Kolmekihilistes struktuurides, milles lõõmutamata ränioksiidi ja hafniumoksiidi kihtide vahele oli lisatud grafeeni kiht, ilmnesid takistuslülituslikud nähtused, kuid selgelt kontrollitavat takistuslülitust ei olnud võimalik nendes esile kutsuda. Kolmekihilistes struktuurides, mille ränioksiidi kihti lõõmutati enne grafeeni kihi lisamist sellele, oli võimalik esile kutsuda hea korratavusega takistuslülitusi. Mäluolekud olid hästi eristatavad, erinedes vooluskaalas ligi kolm suurusjärku, kuid olekud ei jäänud püsima elektrivälja eemaldamisel. Sellest tulenevalt ei saaks neid struktuure paraku rakendada püsimäluna.

Töö tulemusena näidati, et kombineerides omavahel pooljuhtide tehnoloogias kasutatavaid oksiide (TiO_2, Al_2O_3, ZrO_2, HfO_2, SiO_2) ning lisades nendel põhinevatesse mitmekihilistesse struktuuridesse ka grafeeni, on võimalik valmistada uudseid takistuslülituvaid keskkondi ja varieerida nende keskkondade takistuslülituslikke omadusi. Lisaks pakuti välja detailne kirjeldus, kuidas takistuslülitusi esile kutsuda ja läbi viia esmased takistuslülituste mõõtmised uudsetes materjalistruktuurides. Saadud tulemused näitavad, et heade takistuslülituslike mäluomaduste, sh kergesti eristatava takistusolekute erinevuse, lülituste usaldusväärse korratavuse ja erinevate takistusolekute pikaajalise säilivuse, saavutamine vajab selliste struktuuride valmistamisprotsesside edasist optimeerimist ja sobivate materjalikihtide kombinatsioonide hoolikat valimist ja testimist.

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During publishing the results of studies, in the field of RS, which involves two distinct groups of researchers: material scientists and device engineering experts. The former are mainly concerned with the material preparation, while the latter are primarily interested in the reliability of functional devices. This leads to debates and disagreements between the two groups, as they have different perspectives and expectations. As a researcher with an engineering background, I would like to point out that the results obtained by material scientists *de novo* are often preliminary, meaning that they only demonstrate the initial properties and functionality of a material. To achieve the device level, it is necessary to have a deep understanding, thorough development, and optimization of processes,

which are the tasks of device engineers. However, this does not diminish the value of the material scientific approach, as it provides valuable insights into the potential functional materials and their properties. Therefore, in this thesis, I attempted to address both the material science and device engineering aspects of RS.

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PUBLICATIONS

CURRICULUM VITAE

Name	Joonas Merisalu
Date of birth	October 25, 1993
Phone	+372 5855 4730
ORCHID	0000-0001-6498-4588
E-mail	joonas.merisalu@gmail.com

Education:

2018	M.Sc. University of Tartu, Computer engineering and robotics, Tartu, Estonia
2016	B.Sc. University of Tartu, Computer engineering, Tartu, Estonia

Publications included in the thesis:

Merisalu, J.; Arroval, T.; Kasikov, A.; Kozlova, J.; Rähn, M.; Ritslaid, P.; Aarik, J.; Tamm, A.; Kukli, K. (2022). Engineering of atomic layer deposition process for titanium-aluminum-oxide based resistively switching medium. *Materials Science and Engineering B*, 282, 115797. DOI: 10.1016/j.mseb.2022.115797.

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International conferences presentations related to the thesis:

Merisalu, J.; Viskus, T. D.; Aarik, L; Tamm, A.; Kukli, K.; Aarik, J.; Resistive switching in hafnium-titanium oxide thin films grown by atomic layer deposition, 23nd International conference EuroCVD/ Baltic ALD, May, 29–June 2, KU leuven Conference Office, Leuven, Belgium, (2023) P2 (poster presentation)

Merisalu, J.; Otsus, M.; Tarre, A.; Peikolainen, A.-L.; Kozlova, J.; Kukli, K.; Tamm, A.; Bipolar and unipolar resistive switching in hafnium oxide with and without nickel, In; Book of abstracts; AVS 22th International Conference on Atomic Layer Deposition (ALD 2022), June, 26–29, Gent, Belgium, Virtual meeting, 2022, (poster presentation)

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Other publications:

Otsus, M.; Merisalu, J.; Tarre, A.; Peikolainen, A.-L.; Kozlova, J.; Kukli, K.; Tamm, A. Bipolar Resistive switching in hafnium oxide-based nanostructures with and without nickel nanoparticles; *Electronics*, *11*, 2963 (2022)

Kahro, T.; Castán, H.; Dueñas, S.; Merisalu, J.; Kozlova, J.; Jõgiaas, T.; Piirsoo, H.-M.; Kasikov, A.; Ritslaid, P.; Mändar, H.; Tarre, A.; Tamm, A.; Kukli, K.; Structure and behavior of ZrO2-graphene-ZrO2 stacks; *J. Vac. Sci. Technol. A* 38, 063411 (2020)

ELULOOKIRJELDUS

Nimi	Joonas Merisalu
Sünniaeg	25. oktoober 1993
Telefon	+372 5855 4730
ORCHID	0000-0001-6498-4588
E-post	joonas.merisalu@gmail.com

Haridustee:

2018	M.Sc. University of Tartu, Computer engineering and robotics, Tartu, Estonia
2016	B.Sc. University of Tartu, Computer engineering, Tartu, Estonia

Teeside aluseks olevate publikatsioonide loetelu:

Merisalu, J.; Arroval, T.; Kasikov, A.; Kozlova, J.; Rähn, M.; Ritslaid, P.; Aarik, J.; Tamm, A.; Kukli, K. (2022). Engineering of atomic layer deposition process for titanium-aluminum-oxide based resistively switching medium. *Materials Science and Engineering B*, 282, 115797. DOI: 10.1016/j.mseb. 2022.115797.

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