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EFFECT OF ATOMIC LAYER DEPOSITION PARAMETER ALTERATION ON MONOLAYER GRAPHENE AND RESISTIVE SWITCHING

Master's Thesis (30 ECTS)

Curriculum 'Materials Science and Technology'

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Abstract:

This paper is dedicated to the qualitative analysis of monolayer graphene and resistive switching when the parameters of atomic layer deposition, such as temperature and thin film composition, are altered while adding annealing and a buffer layer to the process.

Keywords:

graphene, atomic layer deposition, chemical vapor deposition, Raman spectroscopy, resistive switching

CERCS: P250, P260

AATOMKIHTSADESTAMISE PARAMEETRITE MUUTMISTE MÕJU ÜHEKIHILISE GRAFEENI JA TAKISTUSLÜLITUSTELE

Lühikokkuvõte:

See töö on pühendatud ühekihilise grafeeni kvalitatiivsele analüüsile ja takistuslülitustele, kui aatomkihi sadestamise parameetreid, nagu temperatuur ja kile koostis muudetakse, lisades protsessile lõõmutamise ja puhvrikihi.

Võtmesõnad:

grafeen, aatomkihtsadestamine, keemiline aurufaassadestamine, Raman spektroskoopia, takistuslülitus

CERCS: P250, P260

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TERMS, ABBREVIATIONS AND NOTATIONS

CVD – Chemical Vapor Deposition. Used within this work to grow monolayer graphene.

ALD – Atomic Layer Deposition. Used within this work to grow TiO_2 and TiO_2:SiO_2 thin films.

EBE – Electron Beam Evaporation. Used within this work to grow Au electrodes.

ReRAM – Resistive Random Access Memory. Also known as a memristor.

SEM – Scanning Electron Microscope.

XRR – X-Ray Reflectometry.

sccm – Standard Cubic Centimeters per Minute. It is used to quantify the rate of flow of a fluid under standard conditions.

HEADS - hexakis(ethylamino)disilane, $Si_2(NHC_2H_5)_6$. Used with oxygen plasma to deposit SiO_2 in TiO_2:SiO_2 films within this work.

IPA – isopropyl alcohol, $(CH_3)_2CHOH$. Also known as isopropanol. Its IUPAC name is propan-2-ol.

PMMA – poly(methyl methacrylate), $(C_5O_2H_8)_n$. Its IUPAC name is poly(methyl 2-methylpropenoate). It is a synthetic, transparent polymer which dissolves in organic solvents, used in this work as a protective layer during wet graphene transfer.

1-step ALD – atomic layer deposition process done with a constant temperature.

2-step ALD - atomic layer deposition process done with temperature variation(s). Within this work, the temperature change being from 300 ℃ to 60 ℃ to 300 ℃.

Buffer layer – also known as seed layer or buffering nucleation layer. Used in ALD to protect graphene and promote the growth of a dielectric layer on it.

HRS – high resistance state.

LRS – low resistance state.

INTRODUCTION

Single layer graphene, first isolated from graphite in 2004 by Novoselov *et al.*, had been a grandiose addition to the technological world at a time when the semiconductor industry had been nearing a limit of what silicon-dominated technology could do (Novoselov *et al.*, 2004).

With a thickness of a single layer of carbon atoms formed in a honeycomb lattice, monolayer graphene has nano-scale physical, thermal, mechanical and chemical properties. Its thermal conductivity is 10 times higher than that of copper at around 5×10^3 W/mK, and electron mobility is around 140 times higher than that of silicon at around 2×10^5 cm^2/Vs (Mbayachi *et al.*, 2021). Additionally, graphene does not behave as a metal nor a semiconductor due to having a zero electronic bandgap (Lee *et al.*, 2008). These factors and as well as others combined make graphene one of the most notable nanomaterials with increasing research and development demands (Taghioskoui, 2009).

Within this master's thesis, monolayer graphene has been investigated in conjunction with atomic layer deposition and resistive random-access memory. Graphene was investigated in devices with TiO_2 and TiO_2:SiO_2 mixture thin films, with the following goals in mind:

1. Assessing the quality of graphene covered with a TiO_2 film grown with and without the use of a buffer layer in an ALD process.
2. Assessing the quality of graphene covered with TiO_2 and TiO_2:SiO_2 thin films grown via a 2-step ALD method and with the use of buffer layers.
3. Examining the resistive switching capabilities of functional devices with 2-step ALD layers consisting of different ratios of TiO_2:SiO_2.

The purpose of the first goal is to see the effects of growing ALD thin films onto graphene by growing a TiO_2 layer using a water buffer pretreatment and comparing it to an equivalent graphene with a TiO_2 layer grown without such a buffer.

The second goal is meant to compare the graphene within 1-step devices with top TiO_2 thin films where the entire ALD process was kept at a constant temperature of 300 ℃ and 2-step devices where the top TiO_2 layers were done by heating the device at 300 ℃ for 1 hour, pre-treating at 60 ℃ and growing the thin films at 300 ℃. Additionally, the graphene quality, within the 2-step devices, is assessed for devices containing TiO_2 and three different ratios of TiO_2:SiO_2.

The last goal is to see the resistive switching capabilities of the TiO_2 and TiO_2:SiO_2 2-step devices, with and without graphene, and assess the benefits and detriments of including graphene as well as the effect of TiO_2 and SiO_2 ratio within the dielectric stacks.

1 LITERATURE REVIEW

1.1 Influence of the use of a buffer layer and temperature-step ALD on graphene

With the growth of single-layer graphene, even with a meticulously perfected CVD method there exists the issue of the product containing wrinkles, step edges and defects. Alas, these non-uniformities are the nucleation centres for ALD thin films causing non-uniform deposition of ALD onto graphene. A direct deposition of an ALD film at a constant temperature would result in selective growth of the film onto the graphene non-uniformities, such as defects and edges, due to low probability of the precursors sticking to uniform, non-defective graphene areas.

To avoid the growth of non-uniform ALD layers, a seed layer can be added between the graphene and dielectric layer during the ALD deposition process. Such a seed layer or buffering nucleation layer would enhance the nucleation and growth of the dielectric film on the inert and uniform graphene surface by having the graphene be exposed to a prolonged supply of precursors prior to the deposition itself.

In the buffer layer, water vapour can be used at a low temperature of <50 °C, followed by the growth of the dielectric film at a higher temperature of 200 °C. Such a temperature-step or 2-step deposition alongside the use of a buffer layer could improve the quality of not only the dielectric layer, but also the graphene by protecting it from damages caused by precursors such as ozone. No D band formation could be seen in the Raman spectra (Figure 1, black spectra) of the graphene post-ALD deposition with the use of a buffer layer and 2-step deposition (Rammula *et al.*, 2013) suggesting the graphene remained of a high quality post-deposition of a top-grown dielectric layer.

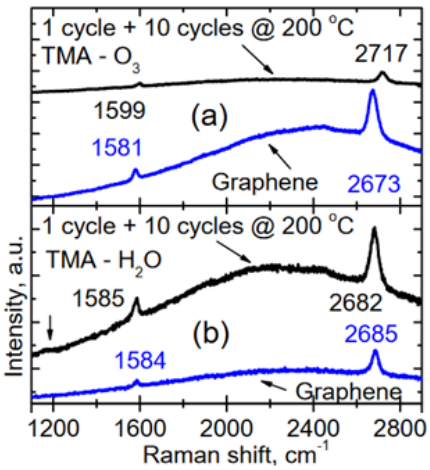

Figure 1. Raman spectra of graphene coated by a dielectric film with a (a) O_3-based and (b) H_2O-based 2-step buffer layer ALD process (Rammula *et al.*, 2013). Blue spectra for graphene prior to top-ALD deposition, black spectra for post-ALD deposition.

Comparatively to the intricate 2-step buffer layer ALD process, a 1-step process tends to cause defects within the underlying graphene layer. As seen in Figure 2, the formation of intense D and D' bands, indicates the presence of defects and decreased structural integrity of the monolayer graphene. This suggests that a good quality graphene layer can be heavily damaged by the addition of a 1-step ALD layer onto it despite the use of a buffer layer (Kahro *et al.*, 2023).

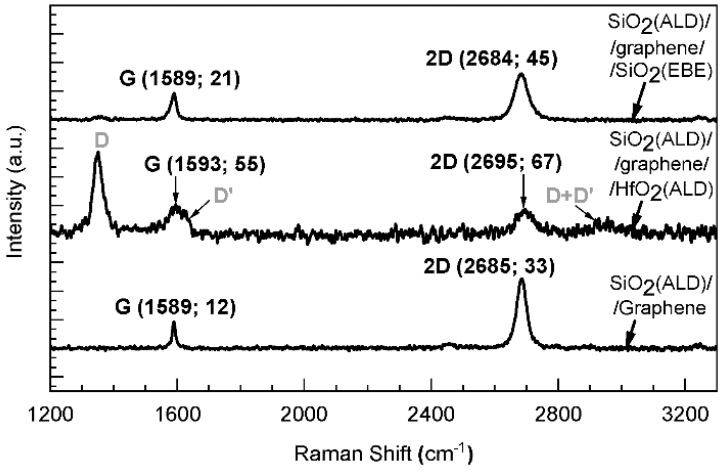

Figure 2. Raman spectra of graphene coated by a dielectric film made with 1-step buffer layer ALD (middle) and the graphene spectra before said deposition (bottom) (Kahro *et al.*, 2023).

Comparatively to the method done by Rammula *et al.*, 2013, the use of a 2-step buffer layer ALD process, where the buffer layer is done at a higher than before temperature of 170 °C seems to result in a similar, mostly undefective, graphene. Despite the presence of a D peak, as

seen on the black spectrum in Figure 3, according to (Alles *et al.*, 2011), the graphene quality does not decrease as drastically as with the addition of a 1-step buffer layer ALD film.

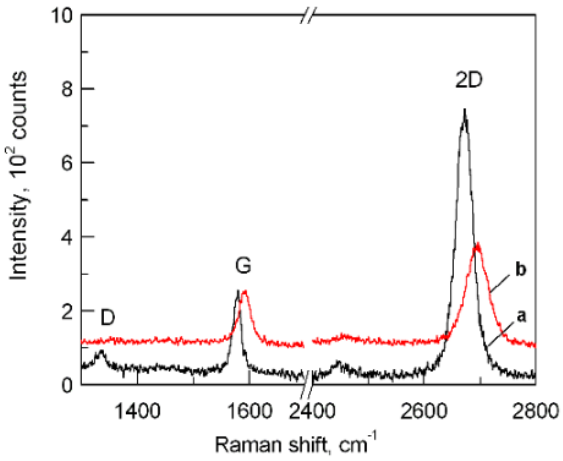

Figure 3. Raman spectra of graphene coated by a dielectric film made with a 2-step buffer layer ALD process (red) and the graphene spectra before said deposition (black) (Alles *et al.*, 2011).

Considering such a drastic change between 2-step and 1-step ALD, such methods of ALD growth onto graphene will be under investigation within this work. Additionally, the need for the use of a buffer layer will be investigated.

1.2 ALD-grown SiO_2 influence on resistive switching and graphene

Within many mixtures, laminates or hybrid structures with quantum dots containing SiO_2, it often enables the resistive switching window to be wider.

Presence of SiO_2 in Fe_2O_3-SiO_2 nanolaminates enables resistive switching and a higher SiO_2 content provides an increased the ratio of LRS to HRS window. The sample with 1.6 ± 0.4 at. % Si (Figure 4a) showed weakly detectable and almost insignificant resistive switching while with an LRS:HRS ratio of 1.4, while the sample with 9.9 ± 1.3 at. % Si (Figure 4b) showed a significant increase in switching capability and an LRS:HRS ratio of 2.6 (Kukli *et al.*, 2020).

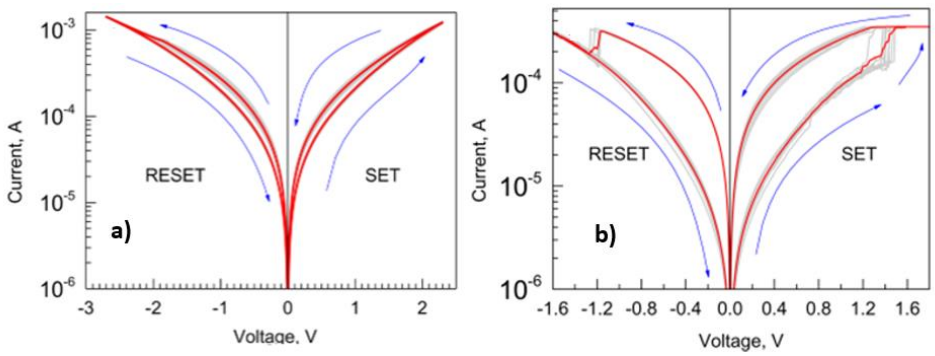

Figure 4. Current-voltage characteristics of nanolaminate films with (a) lower and (b) higher SiO_2 content (Kukli *et al.*, 2020).

Similarly to the effect of SiO_2 in nanolaminates, its presence within a dielectric stack also enhances the resistive switching capability of a device. A switching window of a SiO_2-based device is up to 10^6, alas exhibiting instability and abrupt resets. Comparatively, despite showing relative stability, the switching window of a Al_2O_3 device is only 7 - decreased many-fold compared to the SiO_2-based device. Additionally, by inserting a 20 nm thick SiO_2 layer into the Al_2O_3 device, the switching window was enhanced by 100-fold as well as showed better stability than the SiO_2-based device, and decreased operating voltage and current (Niu *et al.*, 2022).

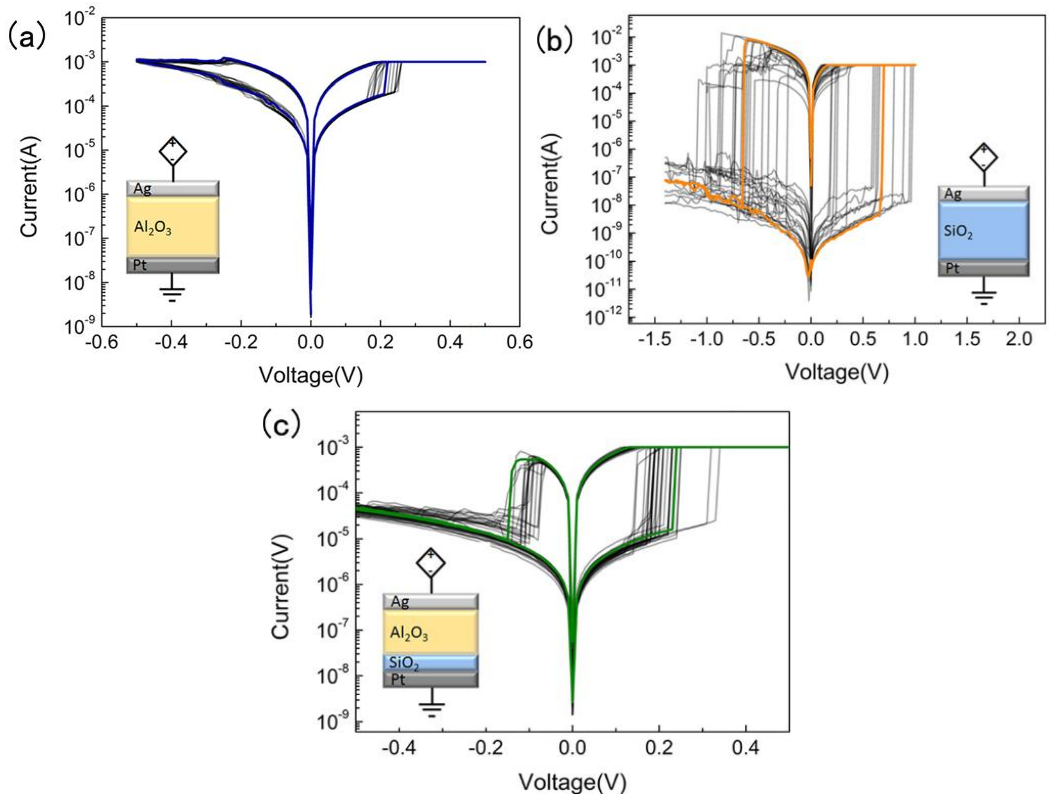

Figure 5. Current-voltage characteristics of (a) Al_2O_3-based, (b) SiO_2-based and (c) Al_2O_3-SiO_2 dielectric stacks (Niu *et al.*, 2022).

While the resistive switching capabilities of a device with only SiO2 ALD films would be great, addition of graphene between two such layers may cause issues.

One of the problems of transferring graphene onto SiO_2 is its poor adhesion and subsequent delamination. The adhesion of graphene to SiO_2 can be insufficient in the wet chemical transfer process, causing water to stay between SiO_2 and graphene, resulting in the graphene breaking during the removal of the protective polymer layer. To counter this, plasma treatment may be

used where the SiO_2 substrate would be treated with Ar^+ or O_2 plasma for a few minutes. With such a treatment, the hydrophobicity of the substrate decreases and the wetting contact angle is increased, permitting uniform drying of the water between SiO2 and graphene and larger scale of graphene transfer. (Lukose *et al.*, 2021).

To make matters worse, due to graphene having a chemically inert surface and lack of surface functional groups, it is challenging to grow ALD thin films onto it. Ozone-assisted growth of ALD films can cause a strong D-band in the Raman spectra, indicating many defects caused by the ALD process. At a temperature as low as 200 °C, the ozone starts reacting with the graphene, introducing an array of defects (Martin *et al.*, 2014). Additionally, unsuccessful attempts at growing SiO_2 via ALD onto graphene had been previously made and resulted in severely damaged graphene with no detectable 2D or G peaks in the Raman spectra, as well as the need to grow the SiO_2 with EBE instead (Kahro *et al.*, 2023).

1.3 Resistive switching dependence on dielectric film crystal structure

Due to the difficulty of using SiO_2 films in graphene-containing dielectric stacks, TiO_2 as well as TiO_2 doped with SiO_2 were instead used in this work. As the dielectric stacks made for the purposes of this work are intended to become resistive random-access memory (ReRAM) devices, the properties of crystal structures in dielectric thin films and the effect on resistive switching performance is discussed. The functionality of ReRAM devices is heavily influenced by phase structure, crystallinity, defect and phase structure (Goren *et al.*, 2014).

TiO_2 can form a crystalline structure consisting of either anatase or rutile phases, or non-crystalline, amorphous phase. When lower than 500 °C deposition temperatures are used, anatase or amorphous TiO_2 thin films are formed (Wetchakun *et al.*, 2012). As the atomic layer deposition temperatures used within this work did not exceed 300 °C, only anatase or amorphous phases could form within TiO_2 and SiO_2-doped TiO_2 thin films.

Amorphous structure of TiO_2 films in ReRAM devices can result in increasingly asymmetric switching and resistance as high as 10^7 to 10^9 Ω in the set-reset cycle (Mähne *et al.*, 2011), with anatase having a lower resistance of 10^5 to 10^7 Ω (Yu *et al.*, 2014). Additionally, compared to amorphous TiO_2, crystalline phases have greater electrical conductivity (Alsaiari *et al.*, 2020) and very low leakage currents at high resistances (Yu *et al.*, 2014). Despite that, Lin *et al.* have shown crystalline dielectric thin films suffering from non-uniform switching performance and higher operating current and voltages, while ReRAM devices with amorphous thin films exhibited uniform switching performance and lower operating voltages (Lin *et al.*, 2013).

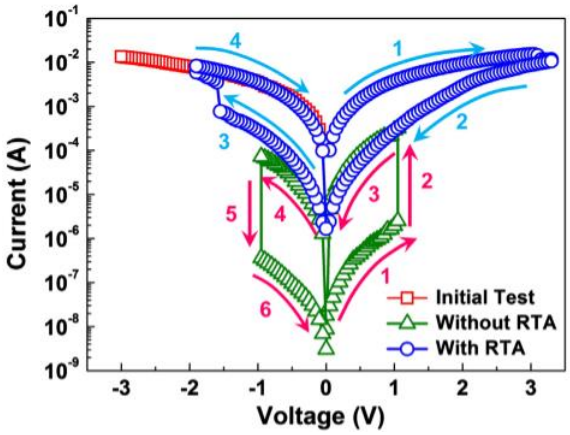

Figure 6. Current-voltage curves of ReRAM devices with (green) amorphous dielectric films and (blue) crystalline dielectric films (Lin et al., 2013).

2 THE AIMS OF THE THESIS

Within this master's thesis, there were three essential goals to be reached:

1. The first experiment aimed to assess the effects of adding a buffer layer to the growth process of the ALD layer directly on top of the graphene in a dielectric stack. The graphene transferred onto TiO_2 thin films would be covered with an identical layer of TiO_2 and compared to a similar stack where the top TiO_2 layer include pretreatment with a buffer layer prior to growth of the ALD layer itself. The addition of a buffer layer to the ALD process could lead to a less defective graphene.
2. The second experiment aimed to compare two different ALD methods, 1-step and 2-step ALD. 1-step ALD would have the TiO_2 thin film grown onto the graphene at a constant temperature, while the 2-step ALD would have the TiO_2 thin film grown onto the graphene while varying the temperature during the process and adding an annealing step. The addition of an annealing step and fine-tuning the temperature during the deposition process could cause the graphene and ALD layers to adhere better, improving the graphene quality underneath the ALD. Additionally, this experiment would involve the assessment of the effect of ALD layers with different TiO_2 and SiO_2 ratios on the quality of graphene. Depending on the results on the first experiment, a buffer layer may be added to the 2-step process if it proves beneficial.
3. The third experiment aimed to use the devices with better graphene quality from the second experiment and compare their resistive switching capabilities to identical devices without graphene. The last experiment would provide knowledge on whether the addition of graphene is beneficial to resistive switching of such dielectric stacks and which TiO_2:SiO_2 ratio is best.

These specific aims were dedicated to the research of monolayer graphene quality and resistive switching of dielectric stacks while modifying ALD composition, growth, and pretreatment parameters. One of the leading hypotheses was that the addition of a buffer layer to an ALD thin film growth process would increase the quality of graphene on top of which such an ALD layer would be grown. The other hypothesis was that the quantity of defects in the graphene under a 2-step ALD layer would decrease and potentially have beneficial effects for resistive switching.

3 EXPERIMENTAL PART

The following chemicals were used within the experiments of this work:

- IPA (>99.5%, Honeywell),
- PMMA (M_w ~996000, Sigma-Aldrich),
- Acetone (>99.8%, Honeywell)
- Acetic acid (99.8-100.5%, Sigma-Aldrich),
- Type II deionized (DI) water,
- Dichloromethane (>99.8%, Sigma-Aldrich),
- Chlorobenzene (>99%, Alfa Aesar),
- Ammonium persulfate (>98%, Sigma-Aldrich).

For the analysis of graphene and ReRAM devices made for the purposes of this work, the following characterisation equipment was used:

- **Raman** analyses were done via a Renishaw inVia micro-Raman spectrometer with a 514 nm laser wavelength and 10%, 50% or 100% laser power. The Raman spectra had been measured at intervals of 1200 to 3300 cm^{-1}. All Raman spectra of graphene had been fitted by the Lorentz function and substrate baselines had been subtracted.
- **SEM** analyses were done via a high-resolution Helios Nanolab^{TM} 600, FEI, to determine the quality of graphene.
- **Electrical characterisation** was done via a source meter Keithley 2636A, and an electrically shielded, light-proof probe station Microtech MPS150.
- **XRR** analyses were done via a SmartLab Rigaku diffractometer, to determine the roughness, density and thickness of the films grown.

3.1 METHODS

Within this work, prior to making layered functional devices, graphene was grown and transferred. For the deposition of monolayer graphene on a copper foil, an in-house-built hot-wall CVD reactor was used at low pressure conditions. It's subsequent transfer onto substrates was done with wet chemical transfer with the use of a protective polymer layer (Li *et al.*, 2009).

To start the graphene production process, a pre-flattened polycrystalline Cu foil was used as a metal catalyst, where the foil being as level as possible ensured the growth of high-quality graphene. The foil was placed into acetone for 5 minutes within an ultrasonic bath for the

removal of residual organic matter, then placed into DI water for another 5 minutes for the removal of residual acetone. The foil was then placed into 20% acetic acid for 10 minutes for the removal of copper oxide, then rinsed with DI water and IPA.

The cleaned and dry foil was placed into a CVD reactor, where the graphene would be deposited onto the foil at 1.5×10^{-2} mbar with the use of Ar, H_2 and Ar/CH_4 (10%) gases. The foil was first annealed at 1000 ˚C for 1 hour in Ar and H_2 gas flow, then a graphene layer was deposited onto the foil within 2 hours of being exposed to Ar/CH_4 gas flow. The gas flow rates used were: 50 sccm of Ar, 10 sccm of H_2, and 30 sccm of Ar/CH_4.

The graphene was then transferred onto desired substrates by having one side of the graphene-covered Cu foil be spin-coated with a protective PMMA layer that had been initially dissolved with chlorobenzene. The uncoated side of the foil would then be etched for 6 minutes with Ar^+ ions in a Femto low pressure plasma system (Diener Electronics). The graphene-Cu foil -etched on one side and protected on the other - was then cut into 5 by 5 cm pieces and left in a 0.1 M ammonium persulfate etchant overnight to etch the copper. After etching of the copper, the pieces were moved to and from DI water multiple times to remove residual etchant and lastly transferred onto substrates. The PMMA was dissolved after transfer by keeping the devices in acetone for 30 minutes (Wang *et al.*, 2021).

The base stack of the substrates used were boron-doped Si wafers with a resistivity of of 0.014–0.020 Ω·cm and a boron concentration of 5×10^{18} to 1×10^{19} cm^{-3}. These Si wafers were pre-covered with pulsed CVD by 10 nm thick nanocrystalline TiN electrode layers using a batch $TiCl_4$/NH_3 process (Granneman *et al.*, 2007; Zagwijn *et al.*, 2008). The TiN was grown at 450 to 500 °C in an ASM A412 Large Batch 300 mm reactor at Fraunhofer IPMS-CNT.

3.1.1 ALD-grown TiO_2 on graphene with and without a buffer layer

TiN-covered Si wafers described previously were the base stack onto which TiO_2 dielectric film, of 6~7 nm nominal thickness, was deposited. Within this part of the experiments, two different versions of TiO_2 layer growth methods were used to deposit it onto graphene, one with the use of a buffer and the other without a buffer layer. The two dielectric stacks can be seen in Figure 7, where on one of the devices an attempt was made to enhance the nucleation and growth of the TiO_2 film on the inert surface of graphene by forming a buffer layer using repeated exposures of precursors beforehand.

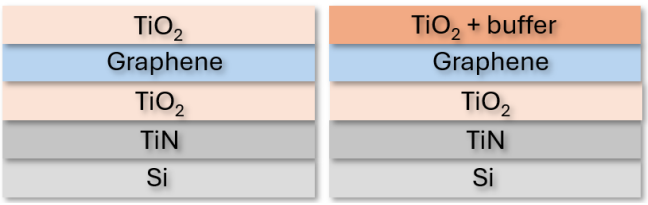

Figure 7. Schematics of the two types of devices designed with the use of a buffer layer (right) and without such a buffer layer (left) during the growth of TiO_2 on graphene.

The TiO_2 layers were grown with the use of titanium tetrachloride, $TiCl_4$, and oxygen plasma, O_2, as precursors at 300 ° C. All ALD films in this work were grown in a commercial Picosun R-200 Advanced ALD system.

In the device where a buffer layer was not applied, 199 ALD cycles were done with pulse and purge time sequences of 0.3–4–15–4 seconds for $TiCl_4$ pulse–N_2 purge–O_2 pulse–N_2 purge lengths, respectively. Both the layer on the base stack and on the graphene were made identically.

In the device where a buffer layer was applied, the buffer was applied by 120 ALD cycles with pulse and purge sequences of 0.1-0.9 seconds for H_2O, followed by the same number of cycles for $TiCl_4$ and again for H_2O. Then, 199 ALD cycles were done with pulse and purge time sequences of 0.3–4–15–4 seconds for $TiCl_4$ pulse–purge–O_2 pulse–purge lengths, respectively.

The graphene quality in both devices was analysed with Raman spectroscopy before and after the deposition of the top ALD layer.

3.1.2 2-step TiO_2 and TiO_2:SiO_2 devices

TiN-covered Si wafers described in section 3.1 were the base stack onto which 1-step or 2-step TiO_2 or TiO_2:SiO_2 dielectric film, of 6~7 nm nominal thickness, was deposited and between which graphene was transferred. In addition to graphene-containing devices, references without graphene were made. Figure 8 shows a schematic of the 8 devices that were made as part of this 2-step ALD experiment.

The devices were made in such a way that the ALD layer below the graphene was grown with a ‘1-step’ method, meaning that it was deposited at a constant temperature, while the top ALD layer was deposited in a ‘2-step’ method, where the temperature was altered twice during the deposition.

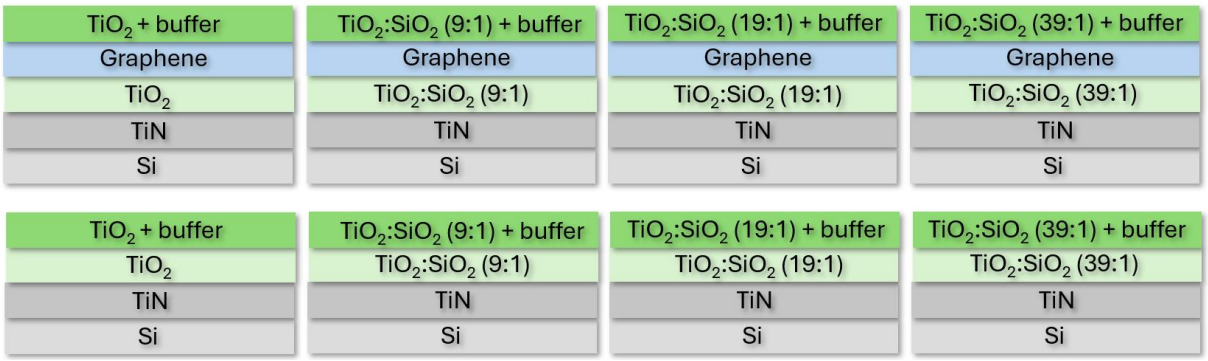

Figure 8. Schematic of two categories of devices: with graphene (top) and references without graphene (bottom) with different SiO_2 content in the ALD layers.

The bottom, 1-step, TiO_2 layer was grown as described in section 3.1.1. for a device without a buffer layer. The top, 2-step, TiO_2 layer was grown such that the device was annealed at 300 °C for 1 hour, followed by a buffer layer deposition at 60 °C. The buffer layer was done as described earlier in section 3.1.1., followed immediately by 19 cycles of the first TiO_2 deposition. Then, at 300 °C, 180 cycles were done of pulse and purge time sequences of 0.3–4–15–4 seconds for $TiCl_4$ pulse–purge–O_2 pulse–purge lengths, respectively.

TiO_2:SiO_2 layers were grown with the use of titanium tetrachloride, $TiCl_4$, and oxygen plasma, O_2, and HEADS, $Si_2(NHC_2H_5)_6$, as precursors at 300 °C. The TiO_2:SiO_2 layers were grown with 9:1, 19:1 and 39:1 ratio of TiO_2 to SiO_2.

The 1-step bottom layer of the 9:1 TiO_2:SiO_2 was grown such that 19 ALD supercycles were done with the deposition formula 19× (1 cycle of SiO_2 + 9 cycles of TiO_2) followed by 19 cycles of TiO_2. Within each TiO_2 and SiO_2 cycle, pulse and purge time sequences of 0.3–4–15–4 seconds were done for $TiCl_4$ or $Si_2(NHC_2H_5)_6$ pulse–purge–O_2 pulse–purge lengths, respectively. For the 1-step 19:1 and 39:1 ratio, their deposition formulas were 9× (1 cycle of SiO_2 + 19 cycles of TiO_2) + 19 cycles of TiO_2, and 4× (1 cycle of SiO_2 + 39 cycles of TiO_2) + 39 cycles of TiO_2, respectively.

The 2-step bottom layer of the 9:1 TiO_2:SiO_2 was grown that the device was annealed at 300 °C for 1 hour, followed by a buffer layer deposition at 60 °C. The buffer layer was done in the same manner as previously mentioned in section 3.1.1., followed by 9 cycles of the first TiO_2 deposition. Afterwards, at 300 °C, the same supercycles as in the 1-step process, resulting in a similar structure. For the 2-step 19:1 and 39:1 ratio, the buffer layer deposition was followed by 19 and 39 cycles of TiO_2, respectively.

The graphene quality in the devices was analysed with Raman spectroscopy before and after the deposition of the top ALD layer. The finished devices were coated with an Au electrode and characterized electrically.

3.2 RESULTS

3.2.1 Buffer layer effect on graphene in TiO_2 grown with 1-step ALD

Two types of devices were made for the purposes of investigating the effect of applying a buffer layer, also known as seed layer, in TiO_2-graphene-TiO_2 stacks deposited and transferred onto a Si-TiN base substrate. The devices in question were Si-TiN-TiO_2-graphene-TiO_2 (no buffer) and Si-TiN-TiO_2-graphene-TiO_2 (buffer) (Figure 7), where both bottom and top TiO_2 layers were grown with 1-step ALD and the top TiO_2 film was grown with or without a buffer layer onto graphene. XRR analysis had been done on ALD-grown layers, where the deposited TiO_2 thin films had been determined to be 9.00 nm thick, in contrast with the nominal 6~7 nm thickness (Appendix 1).

The graphene on both devices had been qualitatively analysed with Raman spectroscopy prior to the deposition of the top TiO_2 layers. It is important to note that the graphene for the TiO_2-graphene-TiO_2 (no buffer) device (Figure 9a) had been slightly damaged during the wet chemical transfer process, resulting in the presence of a D peak on the Raman spectra. There is no apparent D band on the graphene in the device intended for the ALD with a buffer layer (Figure 9b). The height, width and peak positions of the spectra in Figure 9 are noted down in Table 1, where the ratio of I_{2D}:$I_G \geq 2$ shows that the graphene in both devices is predominantly monolayer (Nguyen *et al.*, 2013).

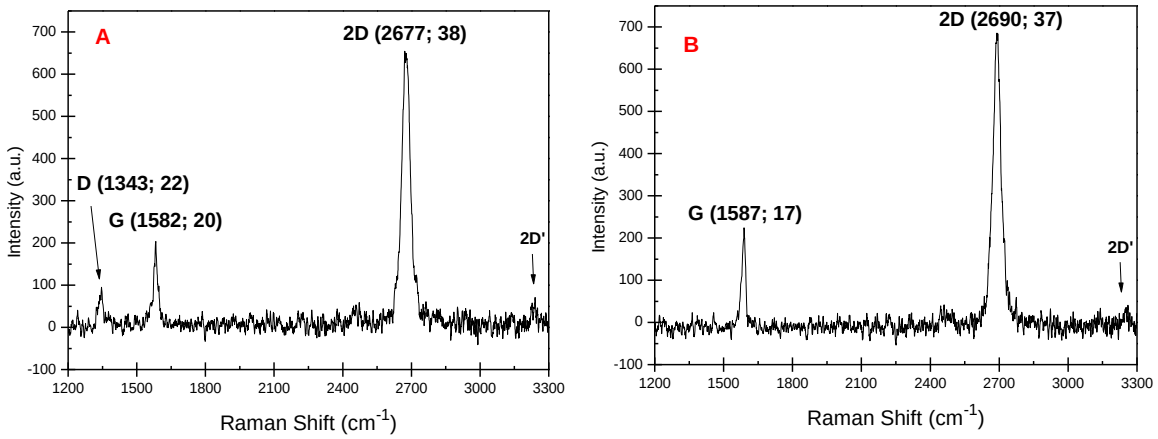

Figure 9. Raman spectra of graphene in (a) Si-TiN-TiO_2-graphene-TiO_2 (no buffer) and (b) Si-TiN-TiO_2-graphene-TiO_2 (buffer) devices prior to the deposition of the top TiO_2 film.

The graphene on both devices had been qualitatively analysed with Raman spectroscopy after to the deposition of the top TiO_2 layers. The graphene in the device where a buffer layer was not used (Figure 10a) had been destroyed, as is apparent from the lack of 2D and G bands. Due to the full destruction of the graphene in the device where a buffer layer was not used during

top ALD deposition, data could not be retrieved for width, height and position of typical graphene peaks.

Comparatively, the graphene had been damaged but not destroyed in the device where TiO_2 was deposited with the use of a buffer layer (Figure 10b). The height, width and peak positions of the spectra in Figure 10 are noted down in Table 2.

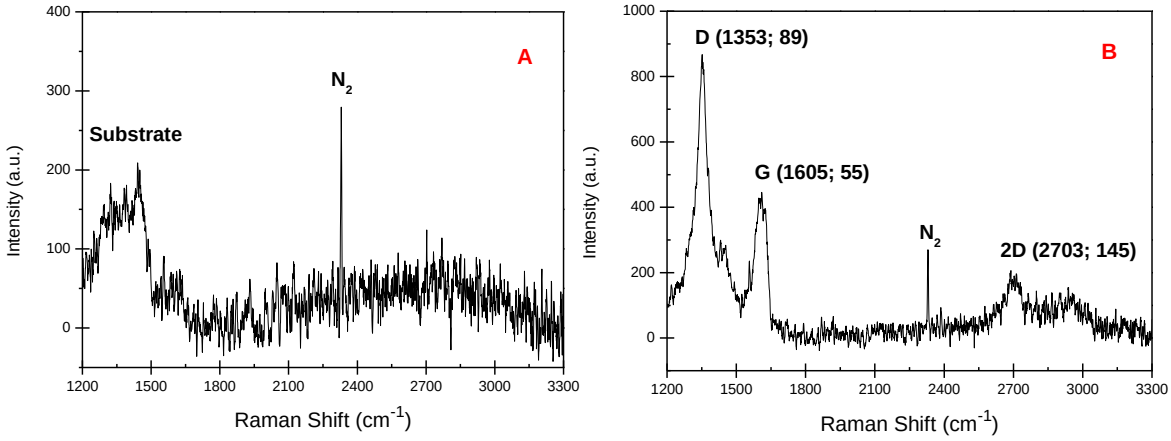

Figure 10. Raman spectra of graphene in (a) Si-TiN-TiO_2-graphene-TiO_2 (no buffer) and (b) Si-TiN-TiO_2-graphene-TiO_2 (buffer) devices after the deposition of the top TiO_2 film.

	ω_{2D}	ω_G	ω_D	$FWHM_{2D}$	$FWHM_G$	$FWHM_D$	I_{2D}	I_G	I_D
Figure 9a	2677	1582	1343	38	21	22	684	181	77
Figure 9b	2690	1587	-	37	17	-	715	231	-

Table 1. Widths, heights and positions of 2D, G and D bands of the graphene in Si-TiN-TiO_2-graphene-TiO_2 (no buffer) and Si-TiN-TiO_2-graphene-TiO_2 (buffer) devices before deposition of top ALD, denoted as Figure 9a and Figure 9b, respectively. All values are in cm^{-1}.

	ω_{2D}	ω_G	ω_D	$FWHM_{2D}$	$FWHM_G$	$FWHM_D$	I_{2D}	I_G	I_D
Figure 10b	2703	1605	1353	145	55	89	150	416	718

Table 2. Widths, heights and positions of 2D, G and D bands of the graphene in Si-TiN-TiO_2-graphene-TiO_2 (buffer) devices after deposition of top ALD denoted as Figure 10b. All values are in cm^{-1}.

3.2.2 2-step ALD effect on graphene in TiO_2 and TiO_2:SiO_2 devices

Two categories of devices were made as part of the second experiment, section 3.1.2, for the purposes of investigating the effect of depositing dielectric thin films grown with 2-step ALD process onto graphene. The devices in question where Si-TiN-TiO_2-graphene-TiO_2 (2-step) and

Si-TiN-TiO_2:SiO_2-graphene-TiO_2:SiO_2 (2-step) of 9:1, 19:1 and 39:1 ratio (Figure 8), where the bottom ALD layers were grown with 1-step processes and the top ALD layers were grown with 2-step ALD processes onto graphene. XRR analysis had been done on ALD-grown layers, where the deposited TiO_2:SiO_2 thin films of 9:1, 19:1 and 39:1 ratio had been determined to be 7.76 nm, 8.51 nm and 8.93 nm thick, respectively (Appendix 2, 3 and 4).

The graphene on the 2-step devices had been qualitatively analysed with Raman spectroscopy prior to the deposition of the top ALD layers. It is important to note that the graphene for the 39:1 ratio TiO_2:SiO_2-graphene-TiO_2:SiO_2 device (Figure 11d) had been slightly damaged during the wet chemical transfer process, resulting in the presence of a D peak on the Raman spectra. There is no apparent D band on the rest of the graphene in the devices intended for the 2-step ALD process with a buffer layer (Figure 11a, b and c). The height, width and peak positions of the spectra in Figure 11 are noted down in Table 3, where the ratio of $I_{2D}/I_G \geq 2$ shows that the graphene in both devices is predominantly monolayer (Nguyen *et al.*, 2013).

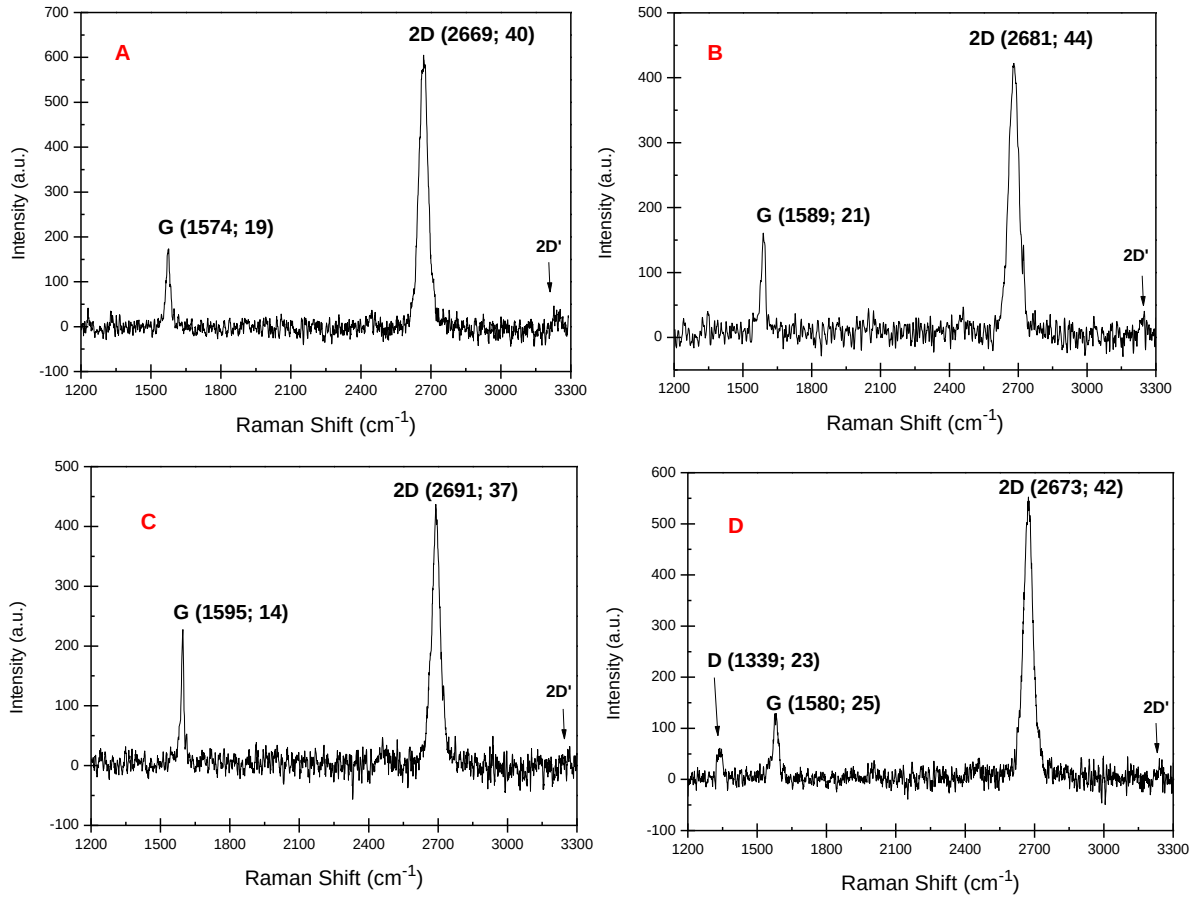

Figure 11. Raman spectra of graphene in devices with underlying dielectric layers of (a) TiO_2, and (b) 9:1, (c) 19:1 and (d) 39:1 ratio of TiO_2:SiO_2, respectively, prior to the deposition of top ALD layers.

Comparatively, the graphene had been damaged in the devices after TiO_2 and TiO_2:SiO_2 mixtures were deposited onto it with the use of a 2-step process and a buffer layer (Figure 12). This is evident by the addition of D bands onto the Raman spectra of TiO_2, as well as 9:1 and 19:1 ratio TiO_2:SiO_2 mixture devices and the slight increase in the width and height of the D band in the 39:1 mixture device. The height, width and peak positions of the spectra in Figure 12 are noted down in Table 4. The defects with the graphene are likely with sp^3- and vacancy-type defects (Eckmann *et al.*, 2012).

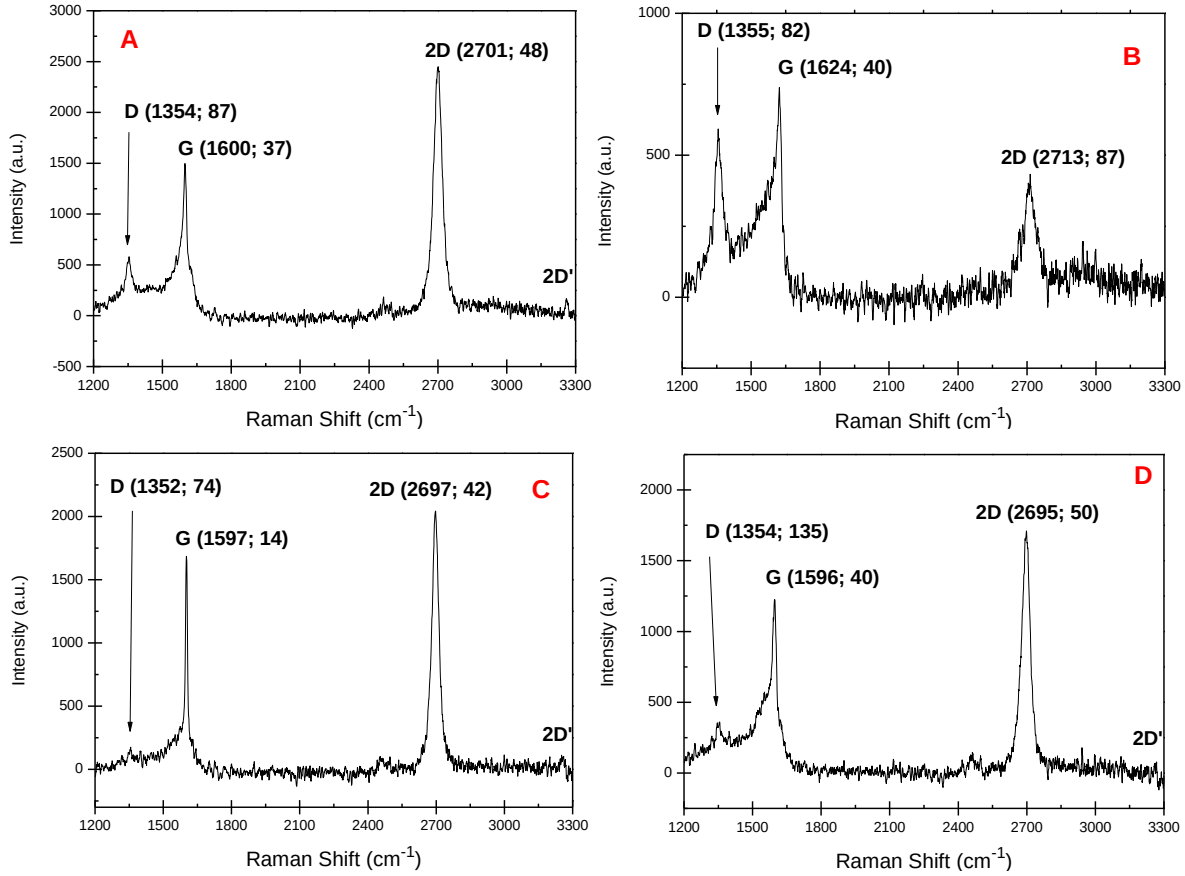

Figure 12. Raman spectra of graphene in devices between dielectric layers of (a) TiO_2, and (b) 9:1, (c) 19:1 and (d) 39:1 ratio of TiO_2:SiO_2, respectively, after the deposition of top ALD layers.

	ω_{2D}	ω_G	ω_D	$FWHM_{2D}$	$FWHM_G$	$FWHM_D$	I_{2D}	I_G	I_D
Figure 11a	2669	1574	-	40	19	-	644	176	-
Figure 11b	2681	1589	-	44	21	-	442	156	-
Figure 11c	2691	1595	-	37	14	-	435	217	-
Figure 11d	2673	1580	1339	42	25	23	565	128	59

Table 3. Widths, heights and positions of 2D, G and D bands of graphene, prior to the deposition of top ALD layer, in devices with underlying dielectric layers of TiO_2 and TiO_2:SiO_2

mixtures with ratios of 9:1, 19:1 and 39:1, denoted as Figure 11a and Figure 11b, c and d, respectively. All values are in cm^{-1}.

	ω_{2D}	ω_G	ω_D	$FWHM_{2D}$	$FWHM_G$	$FWHM_D$	I_{2D}	I_G	I_D
Figure 12a	2701	1600	1354	48	37	87	2587	1563	714
Figure 12b	2713	1624	1355	87	40	82	220	801	401
Figure 12c	2697	1597	1352	42	14	74	2082	1840	308
Figure 12d	2695	1596	1354	50	40	135	1785	1309	541

Table 4. Widths, heights and positions of 2D, G and D bands of graphene, after the deposition of top ALD layer in devices, between dielectric layers of TiO_2 and TiO_2:SiO_2 mixtures with ratios of 9:1, 19:1 and 39:1, denoted as Figure 12a and Figure 12b, c and d, respectively. All values are in cm^{-1}.

3.2.3 Resistive switching of devices with varying SiO_2 and graphene content

Two categories of devices were made with dielectric films done by 2-step ALD, where one part contained graphene between the dielectric layers and the other did not (Figure 8). Both categories contained devices with TiO_2 thin films, as well as TiO_2:SiO_2 mixture films with 9:1, 19:1, and 39:1 ratio.

Figure 13 shows the resistive switching capabilities of graphene-containing TiO_2 and TiO_2:SiO_2 mixture dielectric stacks. The switching current-voltage curves could be repeated for a few cycles in the device with TiO_2, but the switching could not be uniformly reproduced, and the switching window decreased. The switching current-voltage curves could not be repeatedly recorded on the devices with mixture thin films. Devices with higher SiO_2 content produced asymmetric switching curves, while mixture devices with lower SiO_2 content produced small switching windows of less than 1 order of magnitude.

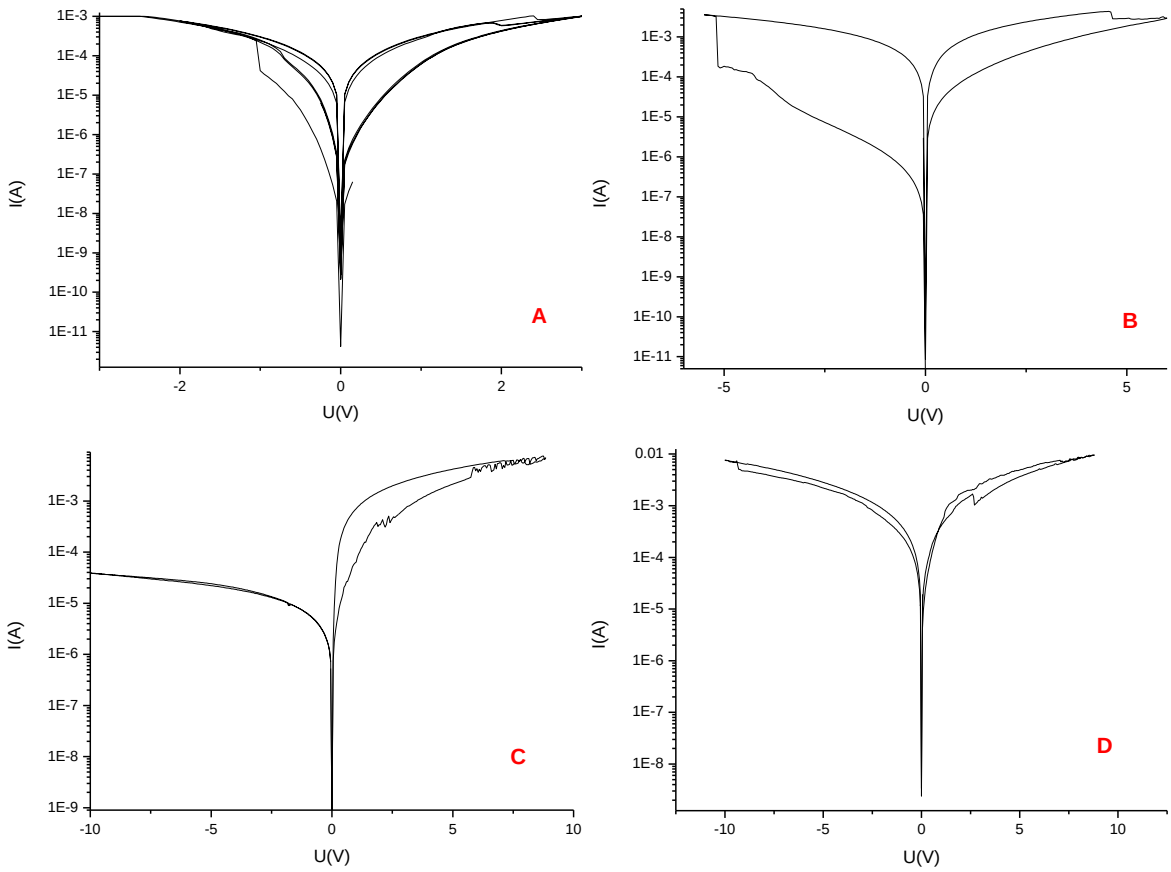

Figure 13. Current-voltage characteristics measured for devices containing graphene between dielectric layers of (a) TiO_2, and (b) 9:1, (c) 19:1 and (d) 39:1 ratio of TiO_2:SiO_2, respectively.

Figure 14 shows the resistive switching capabilities of TiO_2 and TiO_2:SiO_2 mixture dielectric stacks without graphene between the dielectric layers. The switching current-voltage curves could be repeated for tens of cycles in the device with TiO_2, as well as mixture stacks of 19:1 and 39:1 TiO_2:SiO_2 ratio. The switching current-voltage curves could be repeatedly recorded for a few cycles on the mixture device with highest SiO_2 content but was not uniformly reproducible and deteriorated over time. Device with highest SiO_2 content the largest switching window with a maximum of 4 orders of magnitude, while the device with TiO_2 stacks produced a small switching window of 1 order or magnitude.

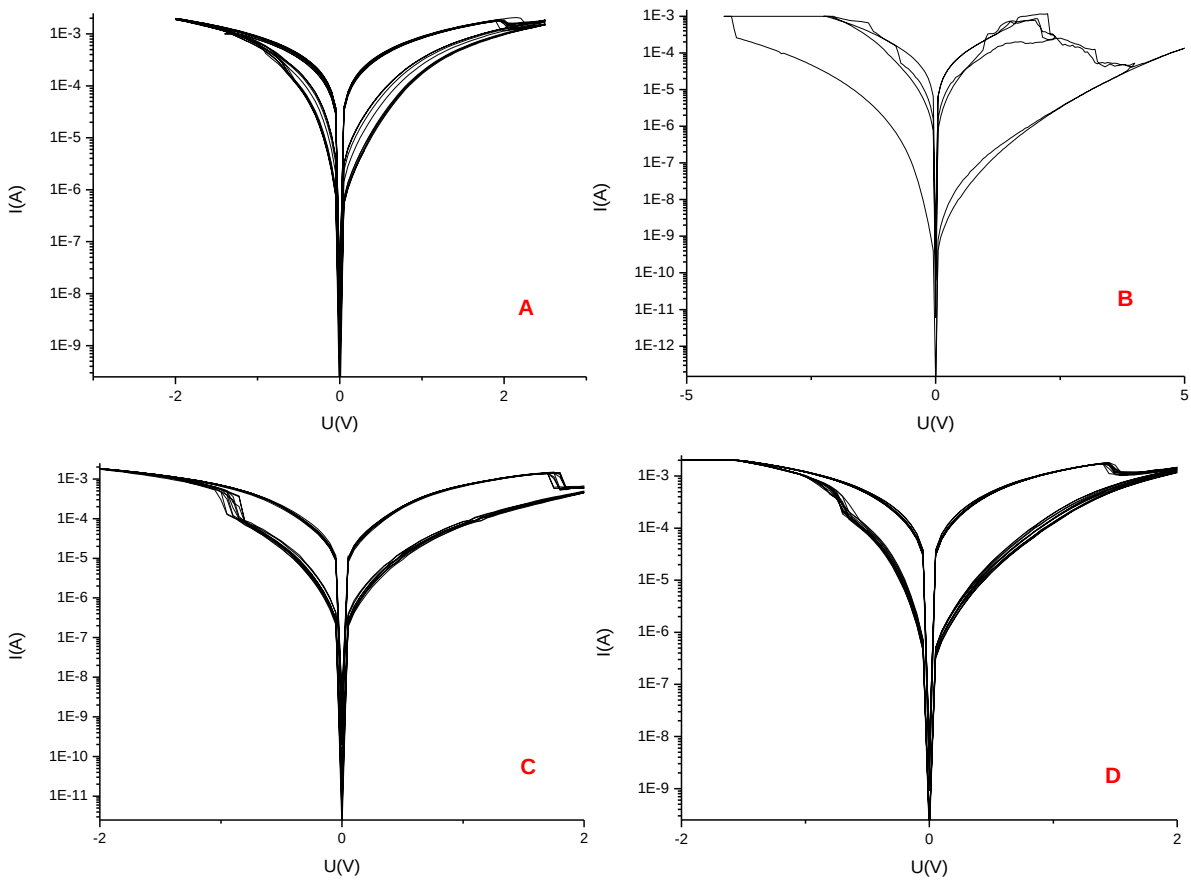

Figure 14. Current-voltage characteristics measured for devices containing no graphene between dielectric layers of (a) TiO_2, and (b) 9:1, (c) 19:1 and (d) 39:1 ratio of TiO_2:SiO_2, respectively.

The crystal structure, namely anatase, presence in the 2-step dielectric layers of the devices was analysed with Raman spectra, where the anatase presence is shown as a peak at approximately 135 cm^{-1} (Su *et al.*, 2008). The anatase crystal structure was present only in the dielectric layer of TiO_2 (Figure 15a).

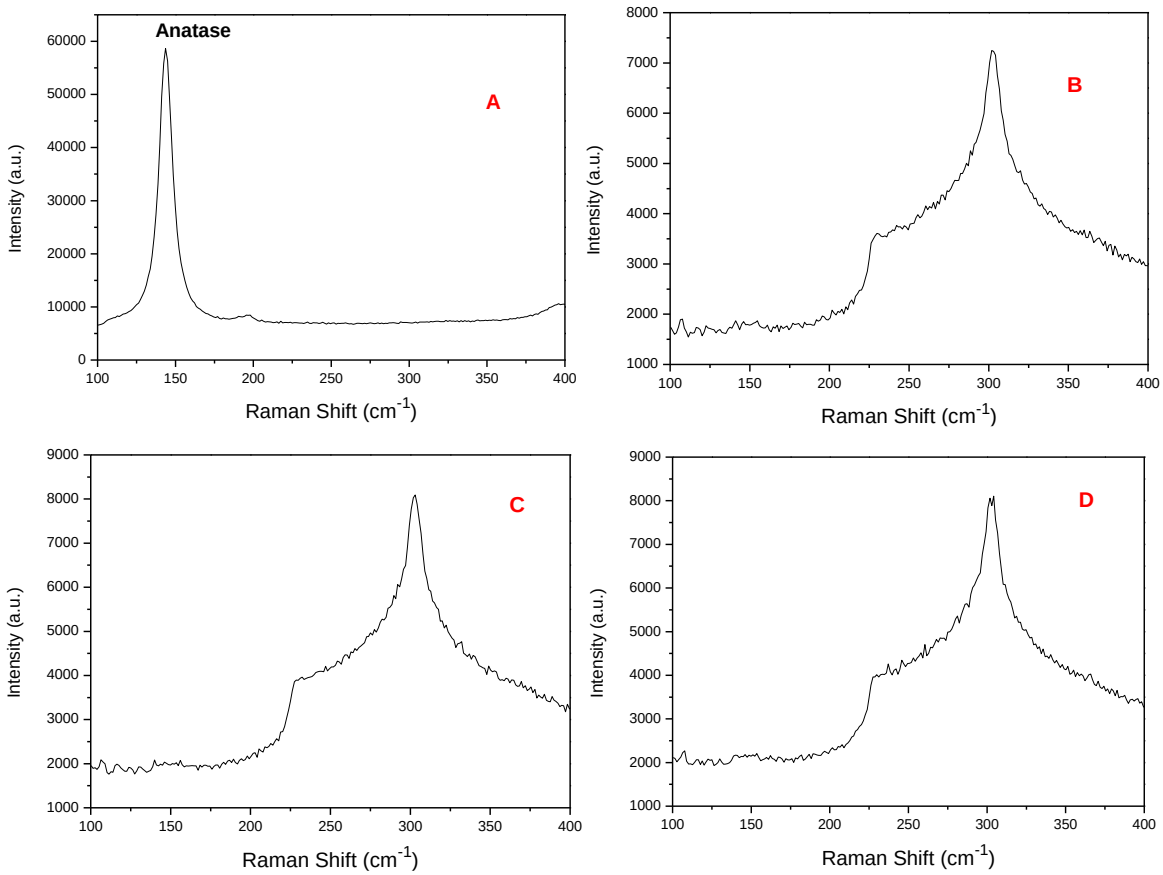

Figure 15. Raman spectra of anatase presence in 2-step (a) TiO_2, and (b) 9:1, (c) 19:1 and (d) 39:1 ratio of TiO_2:SiO_2, respectively.

3.3 DISCUSSION

3.3.1 Choice of dielectric film and 2-step deposition temperatures

Prior to the experiments done within the frame of this work, many attempts had been made to transfer graphene onto devices with ALD-grown SiO_2. Among these attempts, there were many failures, most likely due to the issues discussed in section 1.2, such as the poor adhesion of graphene onto SiO_2 followed by its delamination and the destruction of graphene (Lukose *et al.*, 2021). In few of the transfer attempts, graphene had been transferred with enough of it intact to do further experiments. Thus, attempts were made at producing SiO_2-graphene-SiO_2 stacks, where both SiO_2 films were deposited by ALD.

The deposition of SiO_2 was plasma-assisted instead of ozone-assisted ALD, as the ozone was likely to destroy the graphene (Martin *et al.*, 2014). Upon completion of the stacks, it had been determined through Raman spectroscopy that the graphene had been after the top-ALD process. It is possible that the presence of some defects in the graphene caused by the transfer process, caused the top ALD layer to grow within such defected areas as best nucleation centres, further destroying the graphene (Rammula *et al.*, 2013). Due to such issues with using only SiO_2 with graphene, it was determined that a different ALD thin film was needed. Alas, due to the extraordinary resistive switching capabilities of SiO_2 it could not be fully set aside. Thus, TiO_2 doped with SiO_2 was used instead as well as TiO_2 for the sake of comparison.

Aside from the choice of dielectric film, due to the interest in 2-step ALD processes, a choice had to be made for the temperature variations during the deposition. It had been found, due to prior experiences within the Laboratory of Thin Film Technology in the University of Tartu, that crystalline phases of dielectric films had been preferred in resistive switching and could be beneficial to use within the devices of this work.

As such, different ALD processes had been done to determine the one to be used for the aim of the second experiment within this work. One of such ALD processes included a 2-step buffer layer process at 300/125/300 °C, which yielded the sought-after anatase but produced a defective graphene, evident by the sharp D band (Appendix 5). Another 2-step process without the use of a buffer layer at 300/200 °C yielded a much less defective graphene but also showed no signs of anatase formation within the dielectric layer (Appendix 6), while a 1-step process at 125 °C also yielded no anatase (

Appendix 7).

The process that was deemed to have the best graphene quality while producing anatase within the TiO_2 thin films was done at a temperature variation of 300/60/300 °C. The graphene quality

in the temperature variation experiments suggested that annealing at 300 ℃ and applying a buffer layer at low temperature of 60 ℃, was strongly recommended prior to the deposition of the dielectric layer. The initial annealing at 300 ℃ for 1 hour allowed for the purging of contaminants off the surface of the graphene and improved the adhesion of the oxide layer to the graphene; applying the buffer layer at 60 ℃ allowed for better nucleation and growth of the dielectric on otherwise inert graphene; finishing with the deposition of the dielectric layers at 300 ℃. This process altogether was determined to be the most desired due to producing TiO_2 in the anatase phase (Figure 15a) while keeping the graphene quality high (Figure 12a).

Despite the presence of anatase in TiO_2 films made with the 300/60/300 ℃ 2-step process, it was found that the TiO_2:SiO_2 mixtures did not contain any anatase (Figure 15b, c and d), instead having amorphous structure. Likely different temperature variations are needed to obtain anatase in such mixtures. But, as one of the aims of this work was qualitative analysis of graphene, as well as analysis of the resistive switching capabilities in a device with dielectrics deposited by 2-step ALD, it was best to keep the ALD process the same in all 2-step devices for the sake of comparison.

3.3.2 Buffer layer effect on graphene quality in 1-step ALD

As graphene has been rising in interest in research and development (Taghioskoui, 2009), methods in which it can be added between dielectric films without degradation of its quality are of interest. With such a reason, the need to use a seed layer during deposition of ALD films onto graphene was assessed. With the use of a buffer layer during the dielectric layer deposition, the hope was to maintain the quality of the graphene from before the ALD process.

As seen in Figure 9a, the graphene had been of a decently high quality prior to the top-ALD growth. Its ratio of I_{2D}/I_G being higher than 2, suggested that it was predominantly monolayer (Nguyen *et al.*, 2013), while the I_{2D}/I_G ratio of 3.7 and $FWHM_{2D}$ of lower than 40 suggested a high quality graphene with low amount of defects originating from the CVD process (Kumar *et al.*, 2014).

Figure 9b showed that the 2D peak of the graphene was a similar high quality monolayer graphene, with the I_{2D}/I_G ratio being 3.1 and $FWHM_{2D}$ of 37, prior to the deposition of ALD onto the graphene. Its 2D band lays perfectly at 2690 cm^{-1}, typical to monolayer graphene without defects.

After the deposition of TiO_2 onto graphene, there had been a drastic change between the graphene quality of the device where a buffer layer was applied, and the one without a buffer layer.

Figure 10a showed no signs of graphene remaining after the top-ALD process. Its lack of a 2D and G band, distinct for graphene, was a clear sign that the deposition of a dielectric layer onto graphene without the use of a buffer layer is highly destructive to the integrity of the graphene.

Figure 10b on the other hand showed signs of graphene remaining after the ALD of a dielectric with the use of a buffer layer. It is likely that the graphene contained sp^3-type defects, which would suggest that the carbon atoms within graphene had bonded with out-of-plane atoms, likely from the overlying TiO_2 thin film (Eckmann *et al.*, 2012).

Despite the clearly diminished quality of graphene in the device where a buffer layer was applied, as seen by its high I_D/I_G ratio (Cançado *et al.*, 2011), its quality was significantly better than that of the device where no buffer layer was used and where no graphene could be found. The application of a buffer layer onto graphene enhanced the nucleation of the dielectric layer onto inert graphene and helped keep more of the graphene intact after the deposition.

3.3.3 Comparison of effects of 1-step ALD and 2-step ALD deposited onto graphene

Due to the rising interest in graphene for research and development, it is important to develop better ways of consistently depositing ALD layers onto graphene to form dielectric thin film and graphene stacks, which could be used for example in ReRAM. For this reason 2-step ALD methods with temperature variation have been in development (Rammula *et al.*, 2013). Within this work, such 2-step ALD processes were implemented when depositing dielectric thin films onto graphene, alongside the use of a buffer layer.

As seen in Figure 11, the graphene had been of decently high quality prior to the top-ALD growth. Its ratio of I_{2D}/I_G being higher than 2, suggested that it was predominantly monolayer (Nguyen *et al.*, 2013). For devices with TiO_2 and 9:1, 19:1, and 39:1 TiO_2:SiO_2 mixture layers, the I_{2D}/I_G ratio of 3.7, 2.8, 2.0 and 4.4, respectively, as well as $FWHM_{2D}$ of approximately 40 or lower suggested a high quality graphene with low amount of defects originating from the CVD process (Kumar *et al.*, 2014).

The graphene quality after the 2-step deposition processes onto devices containing different TiO_2:SiO_2 ratio, the Raman spectra were measured and analysed to determine the quality of graphene under the newly deposited dielectric films. As per Figure 12, the lowest quality of

graphene was in the ALD-mixture-containing device where the SiO_2 content was highest at a ratio of 9:1 TiO_2:SiO_2. The Raman spectra shows that this device had the most pronounced, sharp D band and the highest I_D/I_G ratio, pertaining to the highest number of defects present in the graphene post-deposition. Comparatively, the 19:1 and 39:1 TiO_2:SiO_2 devices had low I_D/I_G ratio and a I_{2D}/I_G ratio of more than 1, pertaining that the graphene was still mostly intact. It is important to note that the 39:1 ratio of TiO_2:SiO_2 mixture device had a D band present prior to the top ALD layer deposition, so the more prominent D band does not necessarily mean that the 19:1 mixture device is of better graphene quality. The graphene quality in the device containing TiO_2 thin films had also been of a rather high quality, compared to previous 1-step attempts at maintaining graphene quality, albeit also no longer uniform and defective.

Based on the Raman spectra of graphene in 1-step devices (Figure 10) and the spectra in 2-step devices (Figure 12), the 2-step process is a clear upgrade for the quality of graphene post-overlying ALD. The 1-step buffer layer ALD had resulted in graphene in a large defect amount and very low quality graphene, as per the pronounced D band and high I_D/I_G ratio (Cançado *et al.*, 2011). Comparatively, the 2-step buffer layer ALD resulted in graphene with lower I_D/I_G ratio than that of the graphene in 1-step ALD device, suggesting a lower number of defects in the graphene of devices after 2-step ALD had been used to add a top dielectric layer.

3.3.4 Comparison of the effect of SiO_2 and graphene content on resistive switching

In the present study, resistive switching devices were produced where the dielectric layers were made by 2-step ALD with the use of a buffer layer. The stacks were made with different SiO_2 content, namely with 39:1, 19:1 and 9:1 ratio of TiO_2:SiO_2 as well as TiO_2. Two devices for the four types of stacks were made, where one of each had a graphene layer in between the dielectric layers (Figure 8).

Figure 13 shows that the mixture dielectric stacks containing graphene did not switch repeatedly and operated over unexpectedly high voltages of up to 10 V. The switching was not repeatable in all mixture ratios, was asymmetric and had an LRS:HRS ratio that did not exceed a magnitude of 1 at higher TiO_2:SiO_2 ratio of 39:1 and 19:1, seemingly not working effectively in a ReRAM device (Figure 13c and d). As seen also in the work of (Niu *et al.*, 2022), the higher content of SiO2 in a ReRAM device improved the switching window drastically, from an LRS:HRS ratio of less than 1 to up to 4 (Figure 13d and b, respectively) but at the cost of higher operating power than for TiO_2. Despite the devolving switching capabilities of the mixture devices with higher TiO_2:SiO_2 ratio, TiO_2 did not exhibit the same lack of switching.

Comparatively to the mixtures, the graphene-containing device with TiO_2 stacks had been capable of a few repeated current-voltage cycles, albeit with an unstable, decreasing switching window. Based on only these results of graphene-containing devices, it was initially assumed that mixtures with lower ratio TiO_2:SiO_2 were incapable of switching.

Contrary to the initial assumption from the switching results obtained in the graphene-containing devices, the dielectric stacks without graphene proved to be much more stable ReRAM devices. All devices, except the one with highest SiO_2 content, were capable of tens of repeated SET-RESET cycles and showed high promise at being good ReRAM devices (Figure 14). The current-voltage curves of devices without graphene required lower operating voltages of up to 5 V rather than the 10V in graphene-containing devices. Despite the TiO_2 devices having a small switching window with an LRS:HRS magnitude of 1, the mixtures showed promise at potentially higher switching windows. It could be possible that by fine-tuning the TiO_2:SiO_2 ratio, stable and repeatable current-voltage curves could be obtained while retaining the switching window of 10^4 as in the device with highest SiO_2 content.

Based on the results of the two categories of switching devices, where one had graphene and the other did not, it could be concluded that presence of graphene between the dielectric stacks does not improve the switching capabilities of devices with TiO_2 and TiO_2:SiO_2 thin films.

Additionally, as anatase only occurred in TiO_2 thin films, while the TiO_2:SiO_2 mixtures layers contained no anatase (Figure 15), such difference in crystal structure may be another reason why the graphene-containing ReRAM device with TiO_2 thin films was better capable as cycling between switching, while the devices with TiO_2:SiO_2 mixture layers had failed to cycle. Additionally, unlike in the works of Lin *et al.*, the crystallinity of the TiO_2 thin films did not seem to raise the device operating voltage. It could prove useful to continue the research on the benefits of anatase and amorphous TiO_2 structure in resistive switching but with devices of identical dielectric layers and different crystal structure.

SUMMARY

Based on the results and the discussion section of this thesis, the following conclusions can be drawn about each of the experiments and aims.

In the first experiment, the quality of graphene was assessed when a dielectric layer was deposited onto it with the use of a buffer layer, as well as without such a buffer layer.

Prior to the deposition of a TiO_2 thin film on top of it, the graphene quality had been assessed to be good, with little to no defects present (Figure 9). The deposition of a TiO_2 thin film onto the graphene without the use of a buffer layer during ALD had destroyed the graphene, with the Raman spectra showing no signs of characteristic 2D and G peaks (Figure 10a). On the other hand, the graphene onto which TiO_2 had been deposited with the use of a buffer layer had not been destroyed. The use of a buffer layer showed major improvements to the quality of graphene after deposition of a top ALD layer, seen by the presence of 2D and G peaks (Figure 10b). The carbon atoms within the graphene had likely formed bonds with the overlying dielectric film, resulting in sp^3-type defects (Eckmann *et al.*, 2012). Despite the presence of defects, the use of a buffer layer was deemed necessary in the latter experiments.

In the second experiment, the quality of graphene under dielectric layers done with 1-step and 2-step ALD processes was assessed.

Prior to the deposition of overlying ALD layers, the graphene had been of a high quality and predominantly monolayer, with little to no defects present (Figure 9, Figure 11). After the deposition of 2-step dielectric films onto graphene, the Raman spectra showed a major difference between the quality of graphene under varying ratios of TiO_2:SiO_2 (Figure 12). The Raman spectra showed that the better quality of graphene was in devices of TiO_2:SiO_2 mixtures with higher TiO_2 content, whereas in the mixture device with highest SiO_2 content the graphene had been the most defective, with a very distinct D peak. The graphene likely contained mainly vacancy-type defects in the 9:1 TiO_2:SiO_2 mixture and sp^3-type defects in the 19:1 and 39:1 TiO_2:SiO_2 mixture as well as TiO_2 (Eckmann *et al.*, 2012).

When comparing the graphene under 1-step ALD film versus 2-step ALD films, the latter is a superior method when deposition of dielectrics onto graphene with ALD is involved even when a buffer layer is used in both deposition processes. This is seen by the stark difference between the large, pronounced D band and diminished 2D band in graphene with overlying 1-step TiO_2

Figure 10b) versus the comparatively minor D band and pronounced 2D band in graphene with overlying 2-step TiO_2 (Figure 12).

In the third experiment, resistive switching capabilities of devices made with 2-step ALD were assessed, as well as the presence of graphene between the dielectric stacks of such devices.

Formation and switching in the graphene-containing devices proved difficult. As seen in previously by (Kukli *et al.*, 2020; Niu *et al.*, 2022), the decrease of SiO_2 content in the mixture layers showed a worsening of the resistive switching capabilities of the devices. With the increase of TiO_2:SiO_2 ratio, the LRS:HRS windows became smaller and had less capabilities of switching between SET and RESET states. The mixture devices were unable to continue the switching cycles even at high power (Figure 13b, c and d). If not for this and the asymmetric switching, the mixture with a 9:1 ratio of TiO_2:SiO_2 would have been the best out of the graphene-containing devices, with a maximum window of 10^3. Comparatively, the device containing only TiO_2 was able to repeat the switching cycle at a lower power, albeit in an unstable manner and with a small switching window of 10^1.

In the devices without graphene, the same trend could be seen as in the devices with graphene – the LRS:HRS window increased with the increase in SiO_2 content. The largest switching window with a maximum of 10^4 could be observed in the 9:1 TiO_2:SiO_2 mixture, while the smallest switching window was observed in the device with pure, undoped TiO_2. The devices without graphene showed a capability of switching multiple times without major deterioration in the SET and RESET cycle (Figure 14).

Based on these results, the addition of graphene into such dielectric stacks proved to poorly reflect on the resistive switching capabilities. Devices without graphene were able to more consistently cycle through switching states, had higher stability and less drastic asymmetry. Unlike in the previous work of this author, where the addition of graphene positively affected the switching in SiO_2-HfO_2 dielectric stacks (Kahro *et al.*, 2023), the addition of it between TiO_2 and TiO_2:SiO_2 mixture stacks deteriorated the switching capabilities.

From these results, it seems necessary to further research the effect of graphene in electrical characteristics of dielectric stacks by looking into the effect of uniform versus intentionally defective graphene.

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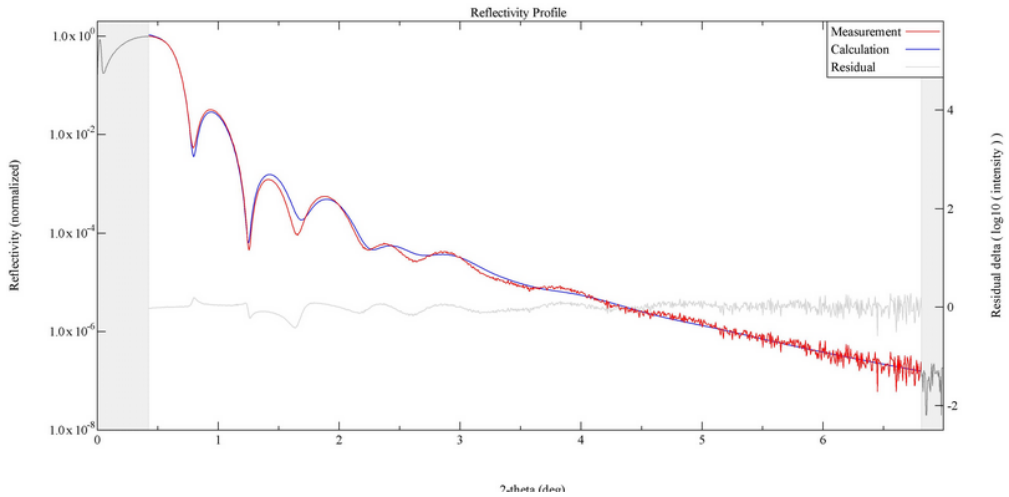
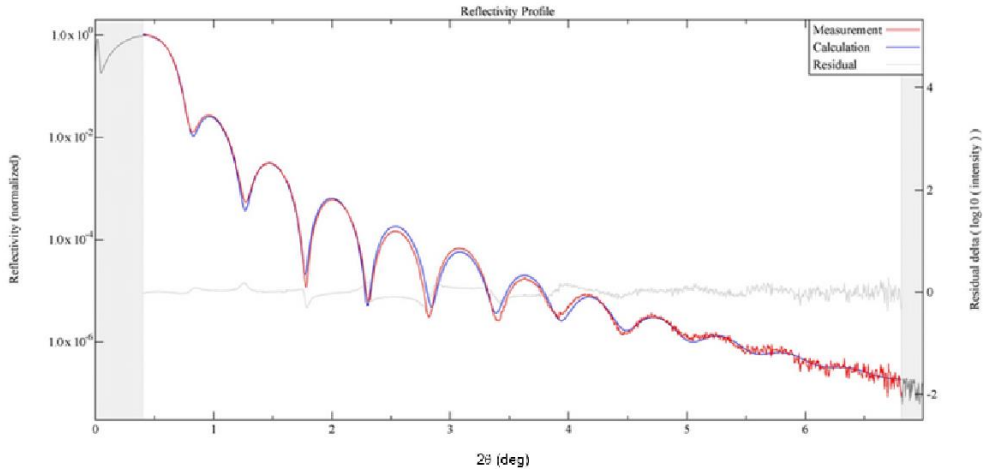
Appendix

ID	Material	Thickness (nm)	Density (g/cm3)	Roughness (nm)
2	TiO2	9.000(3)	3.900(3)	1.3509(18)
1	TiN	7.538(2)	5.05[--]	0.832(3)
Sub.	Si(single)	0.0[--]	2.32919[--]	0.3258(2)



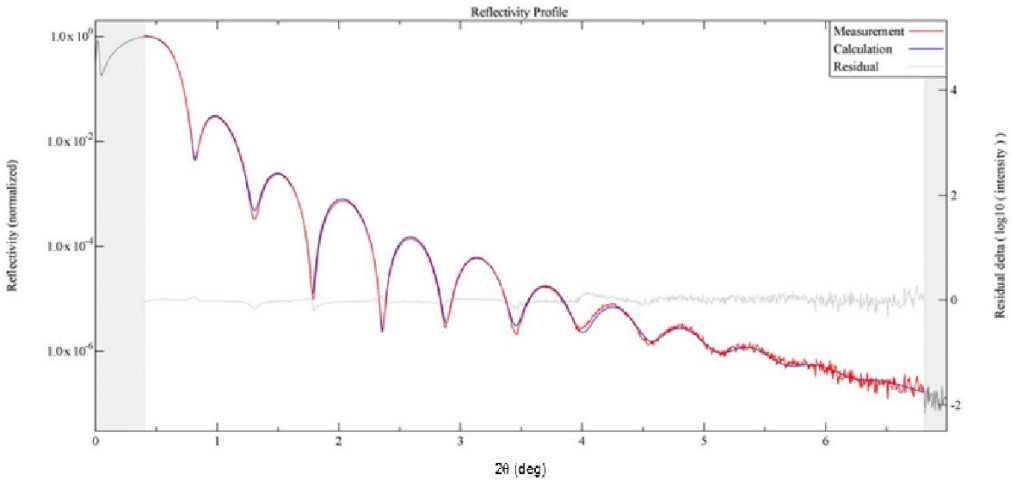
Appendix 1. X-ray reflectivity analysis of a Si-TiN-TiO_2 stack, where the TiO_2 was deposited with 1-step ALD.

ID	Material	Thickness (nm)	Density (g/cm3)	Roughness (nm)
2	TiSiO2	7.76(4)	3.36[--]	0.648(3)
1	TiN	8.16(4)	5.25[--]	1.59(4)
Sub.	Si(single)	0.0[--]	2.32919[--]	0.3272(19)



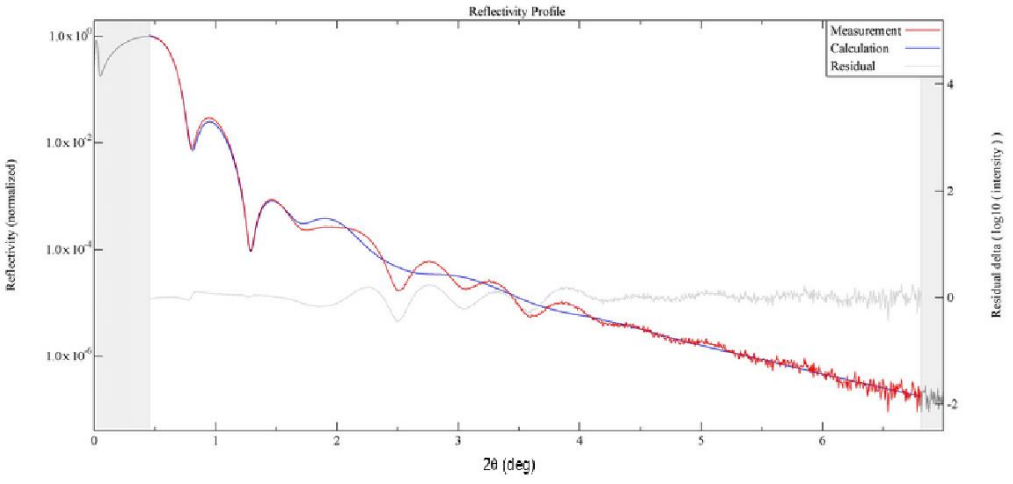
Appendix 2. X-ray reflectivity analysis of a Si-TiN-TiO_2:SiO_2 stack, where the dielectric layer was deposited with 1-step ALD and is of 9:1 ratio.

ID	Material	Thickness (nm)	Density (g/cm3)	Roughness (nm)
2	TiSiO2	8.51(2)	3.751(14)	0.659(2)
1	TiN	7.13(2)	5.2[--]	0.965(11)
Sub.	Si(single)	0.0[--]	2.32919[--]	0.3187(13)

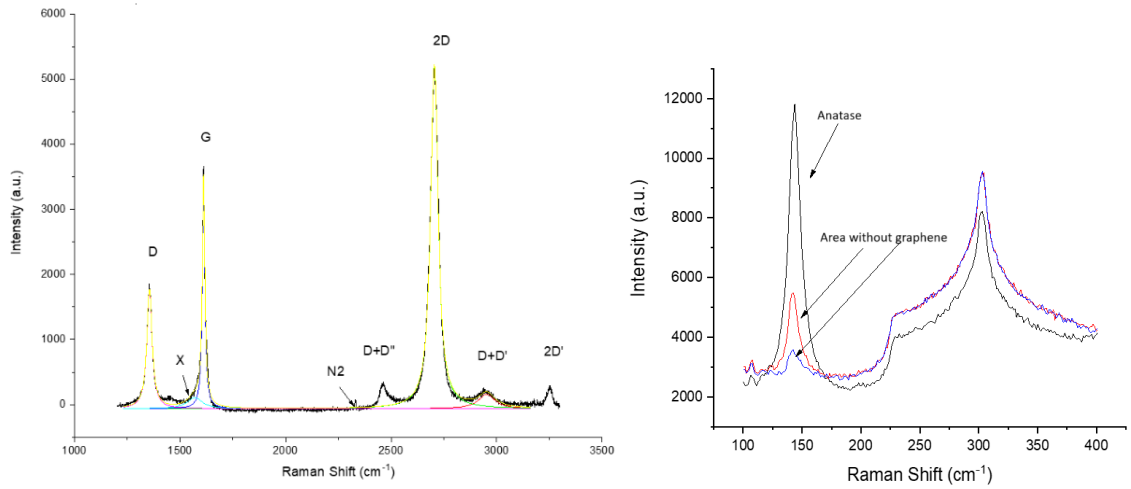


Appendix 3. X-ray reflectivity analysis of a Si-TiN-TiO_2:SiO_2 stack, where the dielectric layer was deposited with 1-step ALD and is of 19:1 ratio.

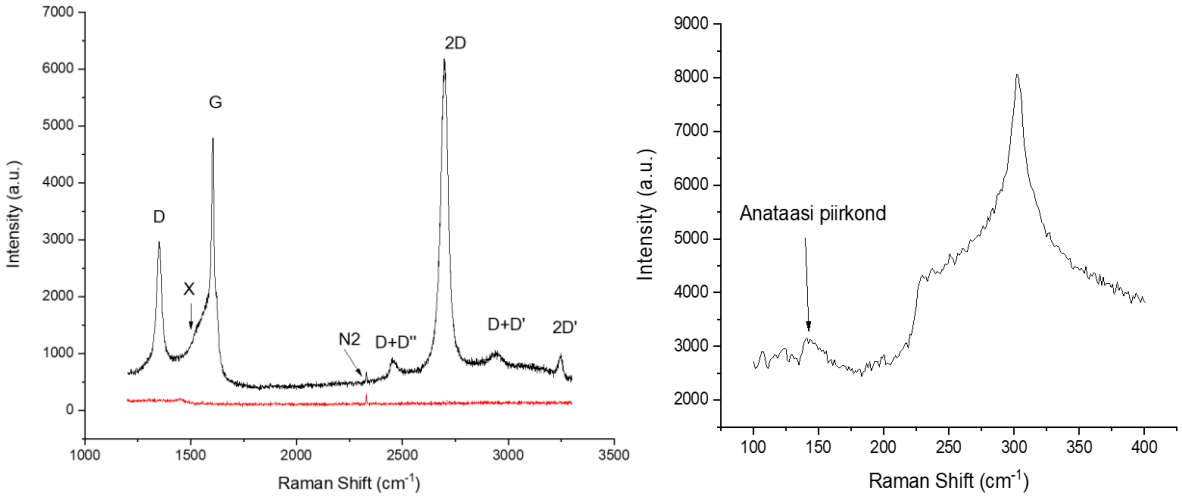
ID	Material	Thickness (nm)	Density (g/cm3)	Roughness (nm)
2	TiSiO2	8.93(4)	3.9[--]	1.71(2)
1	TiN	7.09(3)	5.1[--]	0.84(2)
Sub.	Si(single)	0.0[--]	2.32919[--]	0.309(2)



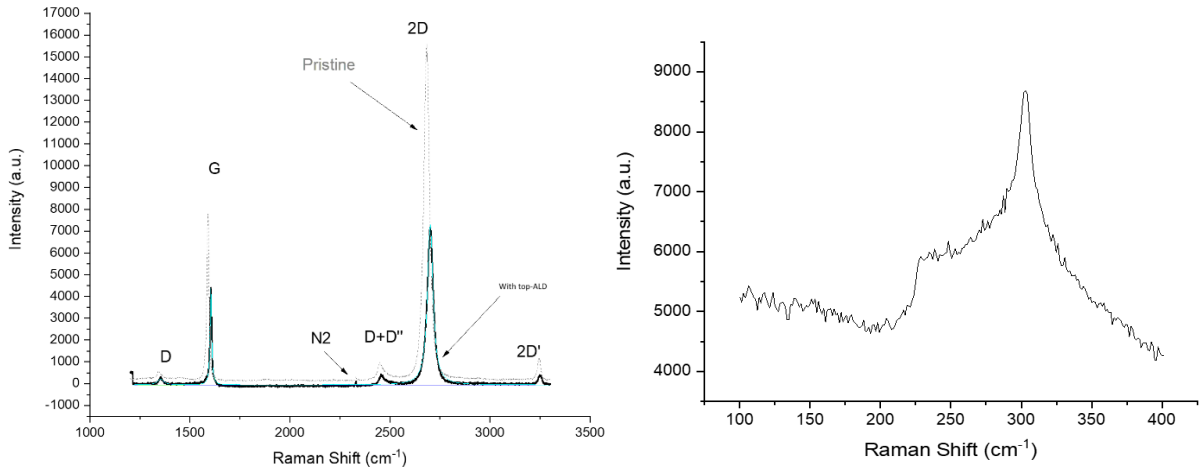
Appendix 4. X-ray reflectivity analysis of a Si-TiN-TiO_2:SiO_2 stack, where the dielectric layer was deposited with 1-step ALD and is of 39:1 ratio.



Appendix 5. Raman spectra of (left) defective graphene made with 300/125/300 °C 2-step ALD of TiO_2 and (right) the anatase crystal structure present in the dielectric but with varying intensity.



Appendix 6. Raman spectra of (left) defective graphene made with 300/200 °C 2-step ALD of TiO_2 and (right) the minor presence of anatase crystal structure in the dielectric.



Appendix 7. Raman spectra of (left) slightly defective graphene made with 125 °C 1-step ALD of TiO_2 and (right) the absence of anatase crystal structure in the dielectric.

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